4th Gen SiC MOSFETs Discrete Package: Characteristics and Precautions for Circuit Design Application Note Rev.001

Note:
The evaluation data and other information described in this application note are the results of evaluation performed by ROHM under identical conditions and presented as references.
We do not guarantee the characteristics described herein.

Contents

1. Introduction

1.1 About this application note

In recent years, SiC MOSFET have rapidly become popular in the field of power electronics. Their advantages in high breakdown voltage and high-speed switching have expanded their application range dramatically. In 2010, ROHM succeeded in the mass production of the SiC MOSFET (planar structure) for the first time in the world. Since then, ROHM has continued the technological innovation as the leading company in the SiC field, including the achievement of a significant shrinkage by employing the trench structure (3rd Generation) in 2015. Recently, ROHM further evolved its own trench structure and started the mass production of the "4th Generation" SiC MOSFET (Figure 1-1).

This application note describes the features of the 4th Gen SiC MOSFETs and explains in more detail how to obtain their maximum performance. Detailed information of the previous generation products is summarized in "SiC Power Device Modules Application Note Rev.003" (*1). In addition to this application note, we provide many technical materials that will help you utilize the SiC MOSFET. (*1 to *21). Furthermore, "ROHM Solution Simulator", which is a web simulation tool supporting the 4th Gen SiC MOSFETs, is publicly available on ROHM's website. Use these resources together with this application note.

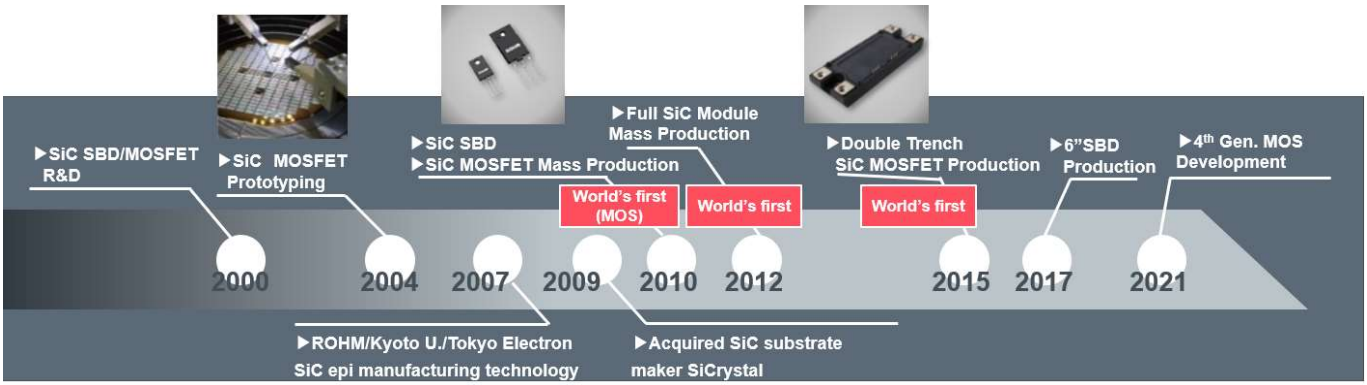


Figure 1-1. Development history of ROHM SiC MOSFET

1.2 Development targets of the 4th Gen SiC MOSFETs

When developing the 4th Gen SiC MOSFETs, we mainly focused on the following three targets.

- Low loss: Realizing industry-leading standardized on-resistance (RonA) and high-speed switching
- Improvement in usability: Realizing the gate drive voltage at 15 V to 18 V without a negative bias
- High reliability: Realizing a high short-circuit rating

First, to achieve the low loss, cell shrinkage for MOSFET and other measures reduced "standardized on-resistance: RonA", which is one of the important indicators, by 40% compared with the 3rd Gen products. Furthermore, the parasitic capacitance was reduced by optimizing the device structure. As a result, the conduction and switching losses have been significantly reduced compared with previous products.

Next, to improve usability, gate driving voltage $V_{G(ON)}$ = 15 V, which is equivalent to that of silicon (Si) MOSFET, has been enabled in addition to $V_{G(ON)}$ = 18 V for the 3rd Gen products. This facilitates replacement of Si-MOSFET with SiC MOSFET, significantly improving the degree of freedom in the circuit design by customers. In addition, to suppress the self-turn-on, the capacitance characteristics of the device is optimized and the gate threshold voltage is designed to be high. Therefore, no negative bias design during turn-off is required. This simplifies the driving circuit while minimizing the circuit scale, leading to cost reduction.

Finally, to achieve high reliability, an actual short-circuit rating greater or equivalent to that of the 3rd Gen products* is acquired even though RonA is reduced (the short-circuit rating is generally decreased as RonA is reduced). This is a very important feature for safely using the SiC MOSFET, which has a high current density per unit area.

(Note: Not guaranteed)

As described above, the 4th Gen products are dramatically improved in the performance, usability, and reliability compared with the previous products. Therefore, we believe the 4th Gen products can help customers solve their design issues. The 4th Gen products not only are offered as discrete or module products, but also can be provided as wafers or chips alone. Please feel free to contact our sales representative for more details including the product lineup.

In the following chapters, we explain the excellent device characteristics of the 4th Gen SiC MOSFETs in more detail.

2. Various characteristics of the 4th Gen SiC MOSFETs

2.1 Standardized on-resistance (RonA)

Since the dielectric breakdown field strength of SiC MOSFET is approximately 10 times higher than that of Si MOSFET, high breakdown voltage can be achieved with a drift layer having a low specific resistance and a thin film thickness. Therefore, compared at the same breakdown voltage, a device with a smaller standardized on-resistance (RonA: on-resistance per unit area) can be realized. As shown in Figure 2-1, when compared at the breakdown voltage class of 650 V, for example, the SiC MOSFET can realize the same on-resistance with a chip size approximately 1/100 and 1/10 of that of the Si MOSFET and the super junction (SJ) MOSFET, respectively. This enables a reduction of the on-resistance with a smaller package as well as gate charge Qg and the capacitance, giving significant advantages in the switching characteristics compared with previous products.

For the super junction MOSFET, the breakdown voltage of existing products is currently only up to approximately 900 V. For the SiC MOSFET, however, a breakdown voltage over 1,700 V can be achieved with a low on-resistance. Previously, the bipolar device structure (having a low on-resistance, but a slow switching) like the IGBT must be employed to support a breakdown voltage over 1,700 V. However, the SiC MOSFET can be used as an excellent device that has a low on-resistance, high breakdown voltage, and high-speed switching simultaneously.

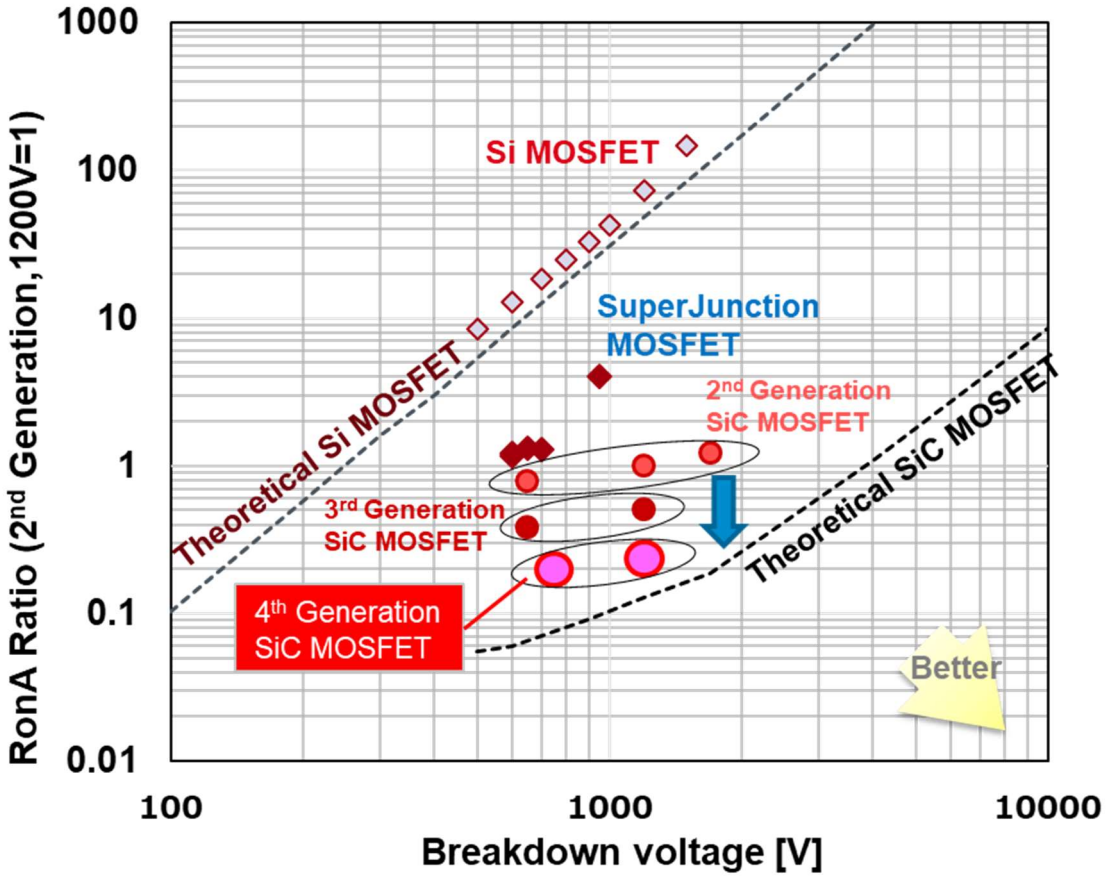
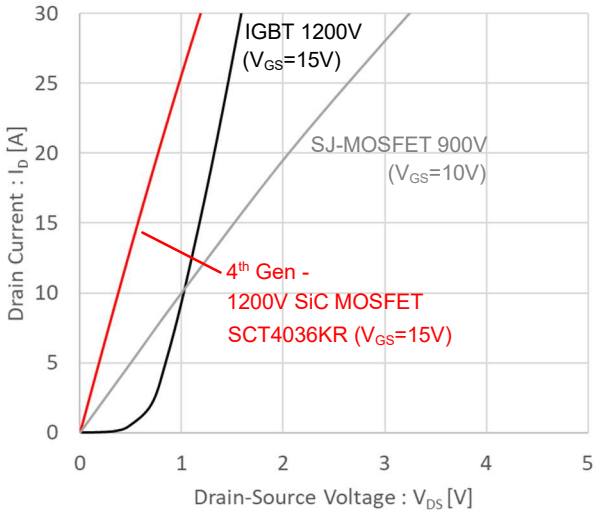


Figure 2-1. Comparison of standardized on-resistance RonA

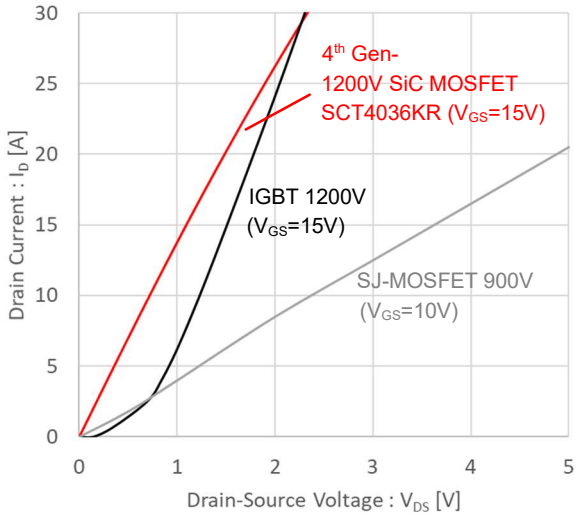
2.2 V_{DS}-I_D characteristics

Generally, since the MOSFET is in the resistive region until it reaches the saturation region, drain-source voltage V_{DS} is generated in proportion to drain current I_D. However, since IGBT has a PN junction, collector current I_c does not flow until the voltage between the collector and emitter (V_{CE}) exceeds the PN junction potential. Therefore, as can be seen in the V_{DS}(V_{CE}) - I_D(I_C) characteristics in Figure 2.2, the smaller the I_D(I_C) is, the smaller the relative conduction loss is in the MOSFET.

Furthermore, when compared with SJ-MOS, the SiC MOSFET can keep the on-resistance low even at high temperature, because not only is its on-resistance low, but also the increase rate of the on-resistance is low against temperature increase. This feature of the SiC MOSFET facilitates the thermal design of circuits. Figure 2-2 shows the V_{DS}-I_D characteristics of the 4th Gen SiC MOSFETs (1,200 V, 36mΩ: SCT4036KR), IGBT, and SJ-MOSFET at ordinary and high temperatures.



(a) Ta=25°C



(a) Ta=150°C

Figure 2-2. V_{DS}-I_D characteristics of various devices (at ordinary and high temperatures)

2.3 Gate drive voltage and on-resistance

The drift layer resistance of the SiC MOSFET is lower than that of the Si-MOSFET. However, since the carrier mobility in the MOSFET channel part is limited by the current level of technology, the channel resistance is higher compared with the Si-MOSFET. Therefore, the on-resistance can be lowered with higher gate voltage V_{GS} (gradually saturated over V_{GS} = 18 V).

Figure 2-3 (b) shows the V_{GS}-$R_{DS(on)}$ characteristics of SCT4026DR, which is the 4th Gen SiC MOSFETs. As can be seen in the figure, the SiC MOSFET is different from general SJ-MOSFET in that its on-resistance varies significantly depending on the V_{GS} value even when the channel is ON. Therefore, increasing the V_{GS} value is effective in fully delivering the performance of the SiC MOSFET by decreasing the on-resistance.

In addition, if the V_{GS} is low, the on-resistance tends to be reduced when the operation temperature is higher. Therefore, make sure that no thermal runaway occurs due to the current being concentrated into a single element, for example, when the elements are connected in parallel and operated at a high temperature and low V_{GS}.

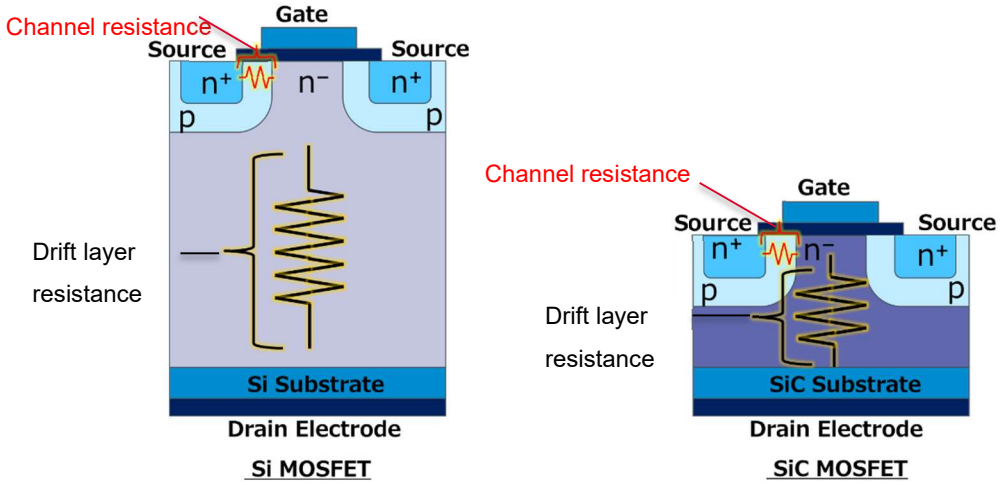


Figure 2-3 (a). Diagram of MOSFET structure

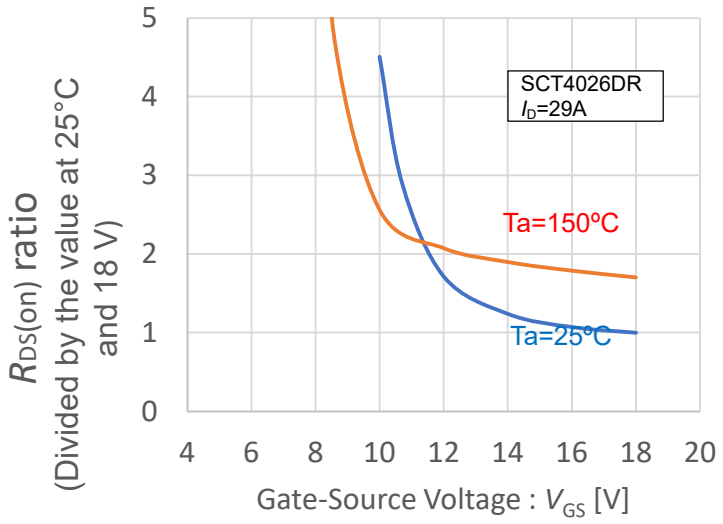


Figure 2-3 (b). V_{GS} - $R_{DS(on)}$ characteristics

2.4 Temperature coefficient of on-resistance

The on-resistance of general SJ-MOSFET significantly increases at high temperature. The reason for this increase is as follows: the resistance component of the drift layer (R_{EPI}), which accounts for 90% or more of the on-resistance of the device, increases by approximately two times when the temperature is increased by 100°C. Although the drift layer resistance of SiC MOSFET also exhibits similar temperature dependence to Si-MOSFET, the increase rate of the on-resistance of the whole device is lower compared with general SJ-MOSFET. This is because the drift layer resistance (partial resistance that increases with temperature) accounts for a small proportion of the whole on-resistance of the SiC MOSFET.

Furthermore, like other semiconductor devices, the temperature coefficient of the on-resistance of SiC MOSFET depends on the breakdown voltage and the device design. For example, for the 750 V product, the temperature coefficient is relatively small because the resistance component of the drift layer is small. For the 1,200 V product, however, the temperature coefficient is larger because the drift layer is thick (i.e., the resistance component is large) compared with the 750 V product. Figure 2-4 shows a graph of the temperature characteristics of the on-resistance, where the X-axis represents the junction temperature (Tj) and the Y-axis represents the on-resistance relative to the value at 25°C. It is shown that, as Tj increases, the relative on-resistance of the 1,200 V product exceeds that of the 750 V product because of the difference in the temperature coefficients.

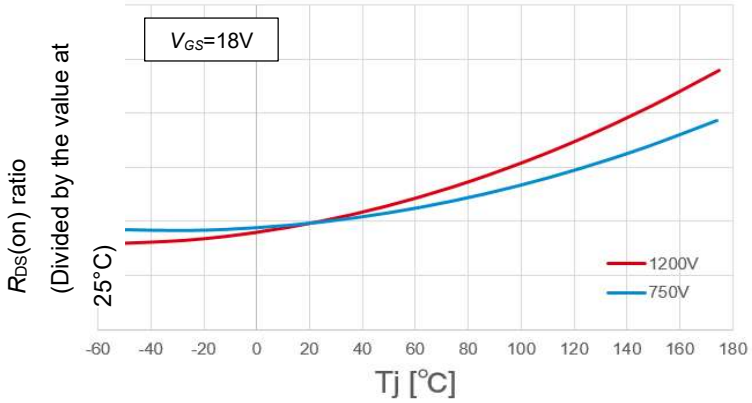


Figure 2-4. Temperature characteristics of standardized $R_{DS(on)}$ of the 4th Gen SiC MOSFETs

2.5 V_{GS}-I_D characteristics

Figure 2-5 shows the V_{GS}-I_D characteristics of SCT4036KR (1,200 V, 36mΩ). The left and right graphs show the same data plotted with the vertical axes in the logarithmic and linear scales, respectively. As can be seen in these graphs, when looking at the values at I_D = 10 mA, the threshold voltage of the 4th Gen SiC MOSFETs is approximately 4 V at room temperature (normally OFF). In addition, the gate voltage required to pass 5 A or greater current is approximately 7 V or greater at room temperature. The threshold voltage generally decreases as the temperature increases. (Tvj: Virtual junction temperature)

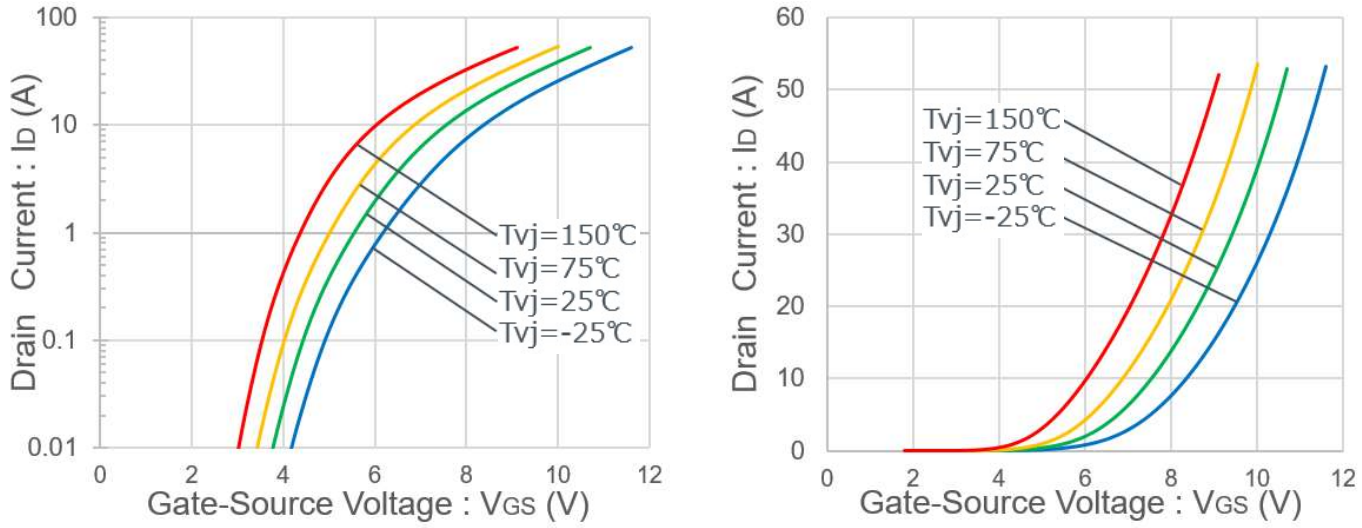


Figure 2-5. V_{GS}-I_D characteristics (SCT4036KR)

2.6 Turn-on/turn-off characteristics

SCT4036KR, which is the 4th Gen SiC MOSFETs, and SCT3040KR, which is the 3rd Gen product in the same on-resistance class, are used to configure each half bridge circuit. Then, the switching characteristics are compared using the inductive load double pulse test (DPT). Figure 2-6 shows the test circuit.

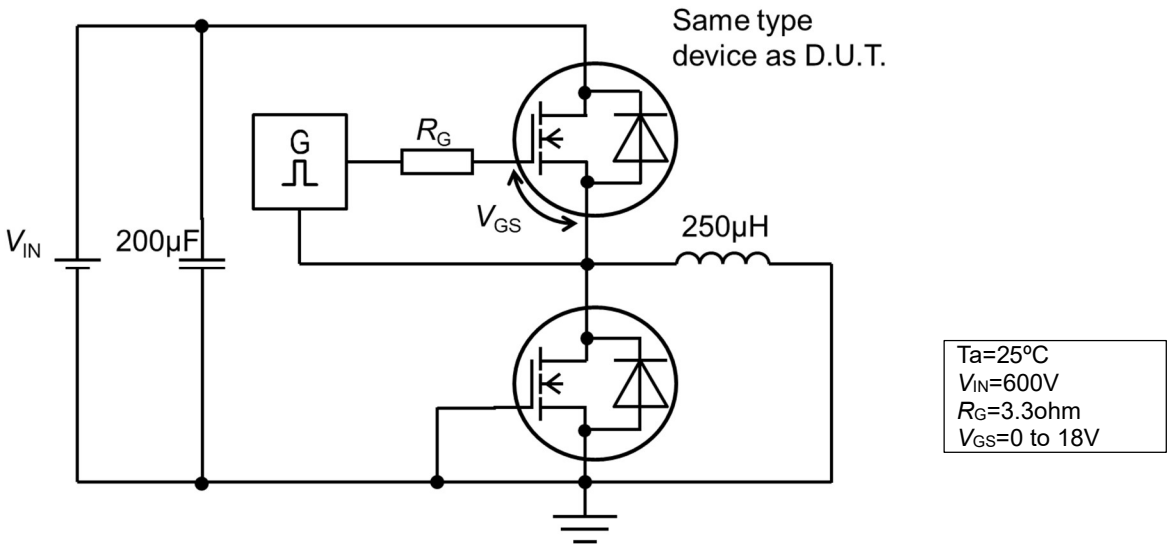


Figure 2-6. Double pulse test circuit

Figures 2-7 and 2-8 show comparisons of the switching waveforms and losses in the double pulse test, respectively (low side). These figures indicate that the switching speed is faster and the switching loss is reduced for the 4th Gen product compared with the 3rd Gen product. These results can be attributed to the reduction in the internal gate resistor value and the capacitance values of C_{oss} and C_{rss} for the 4th Gen products. These values affect the switching speed.

We explain the capacitance and the internal gate resistance in Sections 2-7 and 2-8 in more detail.

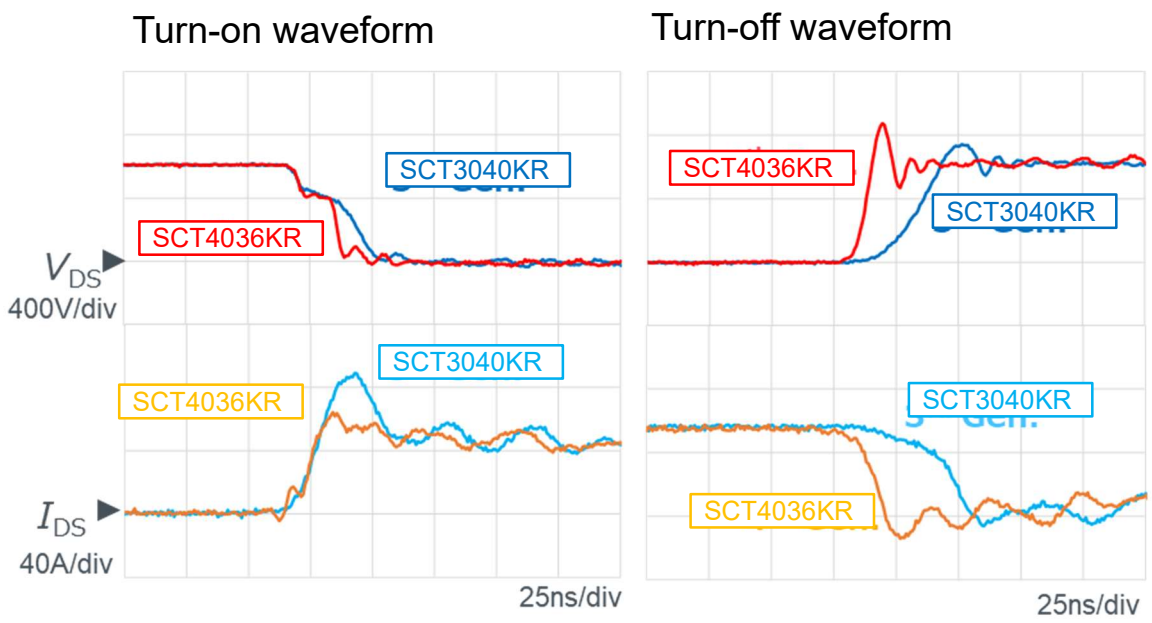


Figure 2-7. Comparison of turn-on/turn-off waveforms

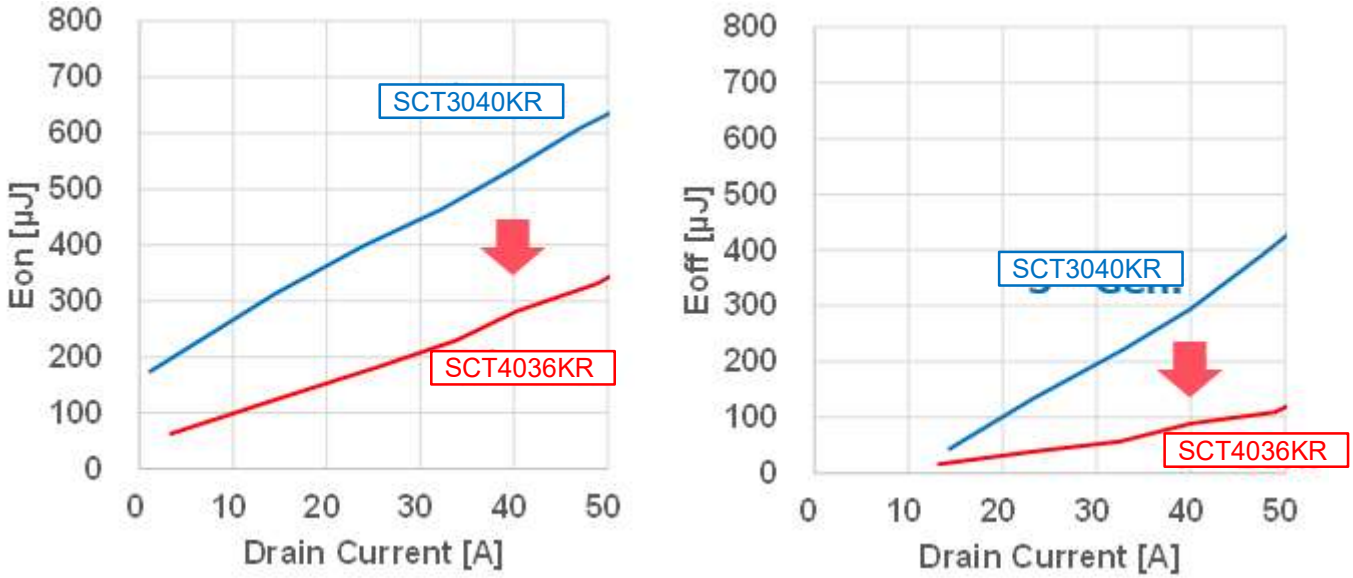


Figure 2-8. Comparison of switching loss

2.7 Capacitance characteristics

As described in Section 2.1, the standardized on-resistance RonA of the 4th Gen products is significantly reduced compared with the 3rd Gen products. This allows downsizing of elements for the 4th Gen products compared with products with equivalent on-resistance. Parasitic capacitances C_{oss} and C_{rss} are generally decreased as the element size is decreased in SiC MOSFET (Figure 2-9). As a result, the switching speed is improved as described in Section 2.6.

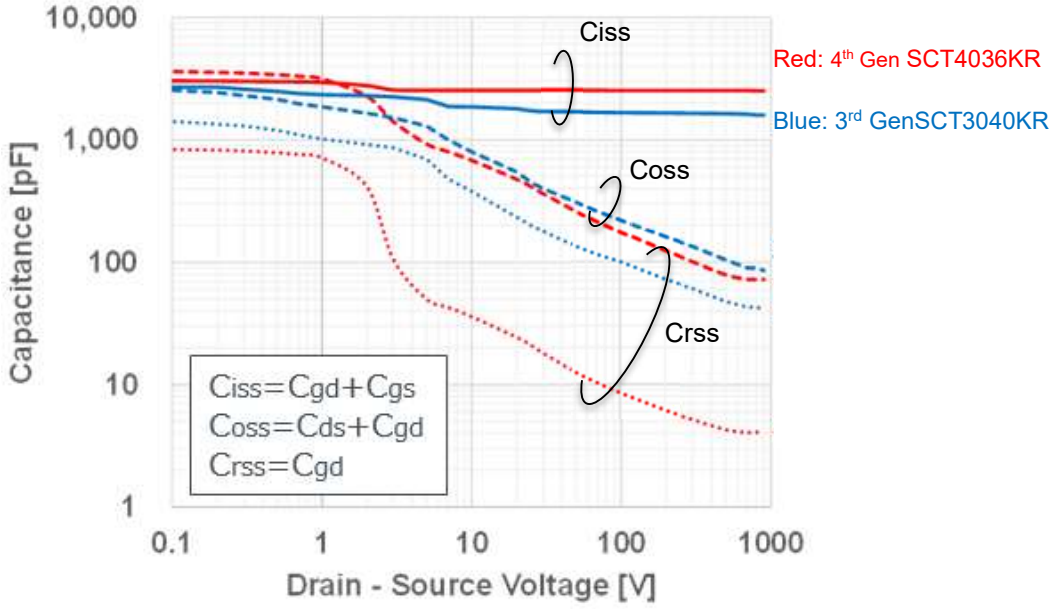


Figure 2-9. Comparison of capacitance between 4th Gen and 3rd Gen

Furthermore, for the 4th Gen products, not only the capacitance values of C_{oss} and C_{rss} are simply reduced, but also the ratio of capacitances C_{rss}/C_{iss} is significantly reduced (Figure 2-10). This results in reduction in the risk of occurrence of the self-turn-on, which may cause problems during switching at a high speed.

Figure 2-11 shows the schematic diagram of the self-turn-on. If a steep dv/dt occurs between the drain and source of MOSFET in the OFF state, for example, during a switching process, voltage corresponding to the ratio of parasitic capacitances C_{gd} and C_{gs} (approximately the capacitance ratio of C_{rss} and C_{iss}) is induced between the gate and the source. At this time, if the gate-source voltage exceeds threshold voltage Vth, the MOSFET is turned ON by error. This phenomenon is referred to as the self-turn-on.

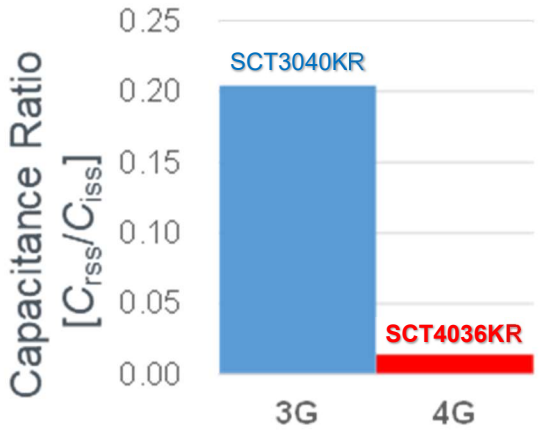


Figure 2-10. Reduction in capacitance ratio C_{rss}/C_{iss}

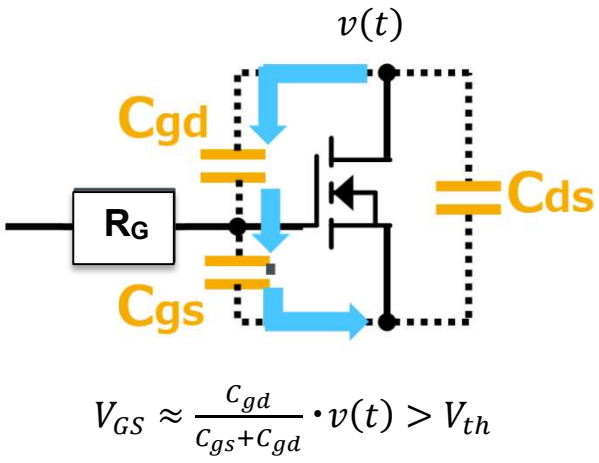


Figure 2-11. Self-turn-on phenomenon

2.8 Internal gate resistance

If the elements have the same structure, the element with a smaller size generally has a higher internal gate resistance. However, although the elements of the 4th Gen products are downsized compared with the 3rd Gen products, the internal gate resistance of the 4th Gen products is significantly reduced (approximately to 1/6) by optimizing the wafer processes and the element patterns.

As shown in Figure 2-12, to drive the gate of the MOSFET, an external gate resistor (R_{G_EXT}: for surge adjustment, etc.) and an internal gate resistance (R_{G_INT}: specific to the gate wire resistance and other factors on the element) are connected in series between the gate driver and the gate oxide film. Therefore, the switching speed is faster and the switching loss is smaller as the sum of R_{G_EXT} and R_{G_INT} is smaller.

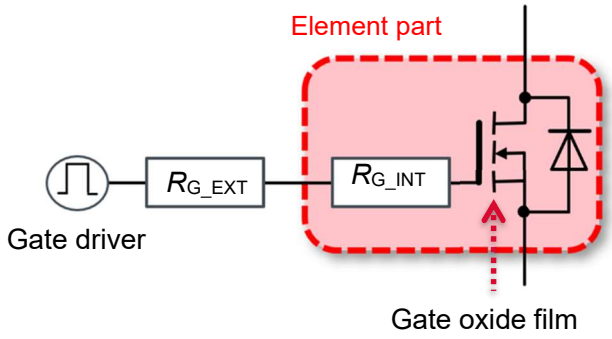


Figure 2-12. External gate resistance R_{G_EXT} and internal gate resistance R_{G_INT}

Next, Figure 2-13 shows a comparison of the switching loss between the 4th Gen and 3rd Gen products with varied external gate resistance R_{G_EXT}. The evaluation method is the double pulse test as described in Section 2.6. As can be seen in the figure, even if driven with the same R_{G_EXT}, the switching loss can be significantly reduced for the 4th Gen products. As described in Section 2.7, this can be attributed to a smaller parasitic capacitance and internal gate resistance R_{G_INT}, smaller sum of the gate resistances (R_{G_INT} + R_{G_EXT}), and increase in the switching speed for the 4th Gen products.

Furthermore, since the switching speed is determined from the sum of R_G (R_{G_INT} + R_{G_EXT}), decrease in R_{G_INT} extends the adjustment range of R_{G_EXT}. Therefore, flexible measures can be taken for suppression of the gate surge, improvement of the switching characteristics, etc. This can be considered another important feature of the 4th Gen products.

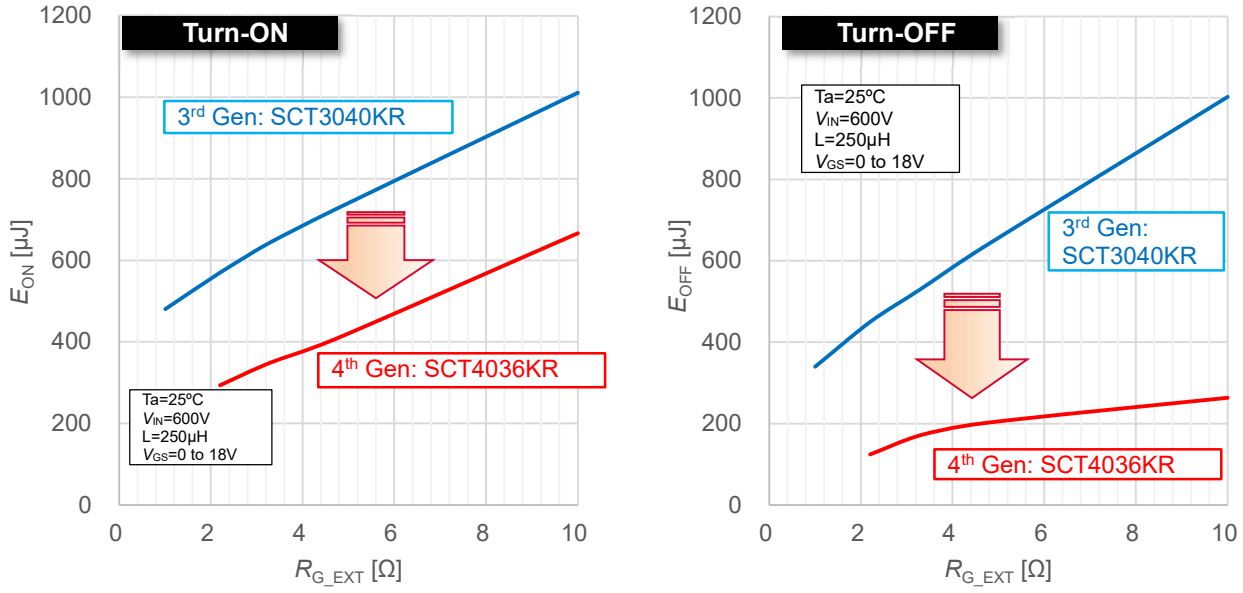
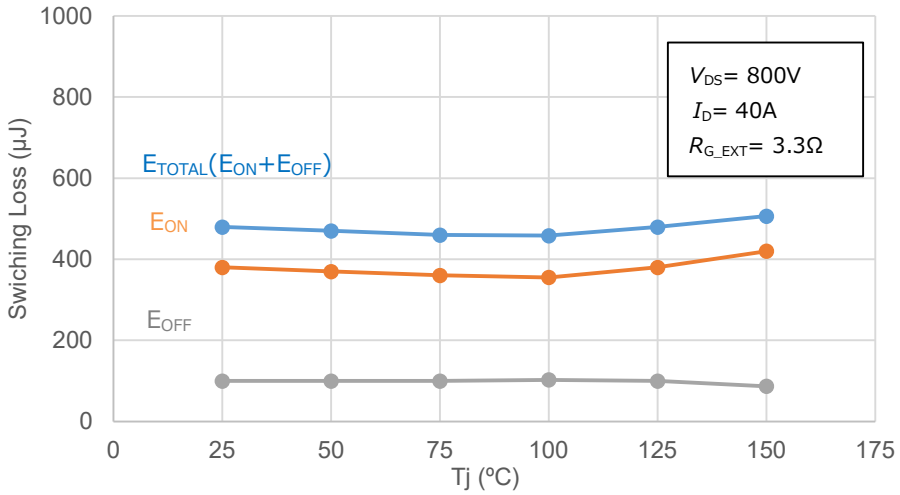


Figure 2-13. Comparison of R_{G_EXT} dependence of switching loss (4th Gen vs.3rd Gen products)

2.9 Temperature dependence of switching characteristics

While the switching speed of semiconductor devices generally depends strongly on the parasitic capacitance, the parasitic capacitance of the SiC MOSFET shows little change against temperature. As a result, the temperature characteristics of the switching loss are also extremely stable. Figure 2-14 shows the temperature dependence of the switching loss of SCT4036KR, which is the 4th Gen SiC MOSFETs. As can be seen in the graph below, the characteristics of the switching loss are nearly flat against the change in temperature.



2.10 Recovery characteristics of body diode

Figure 2-15 shows a comparison of the recovery characteristics of the body diodes in the 4th Gen and 3rd Gen products. As described in the section “2.8 Internal gate resistance”, the switching speed of the 4th Gen products is increased by reducing the internal gate resistance compared with the 3rd Gen products. As a trade-off, the recovery characteristics generally deteriorate due to increase in surge. However, the graph shows that little recovery current flows for the 4th Gen product although the switching speed is increased. This result indicates that the 4th Gen products can contribute to a significant reduction in the switching loss in various bridge circuits where recovery current may occur, including totem-pole PFC and inverters. Furthermore, reduction in the failure risk and noise caused by the recovery current can also be expected.

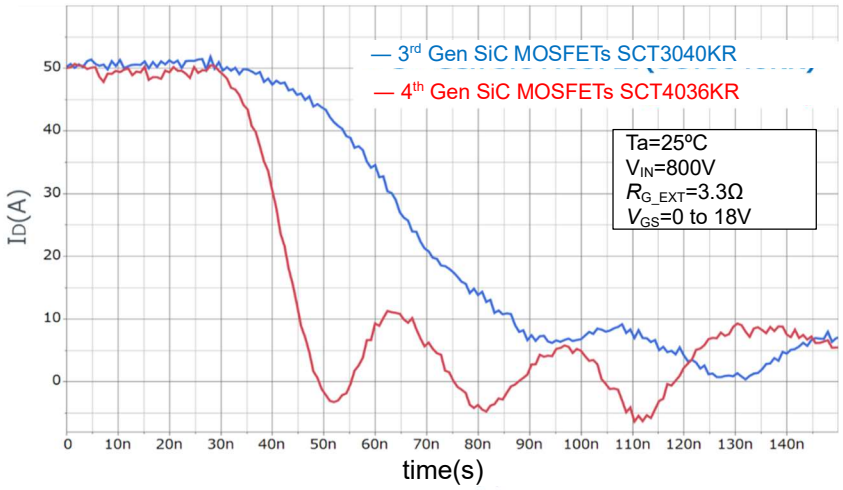
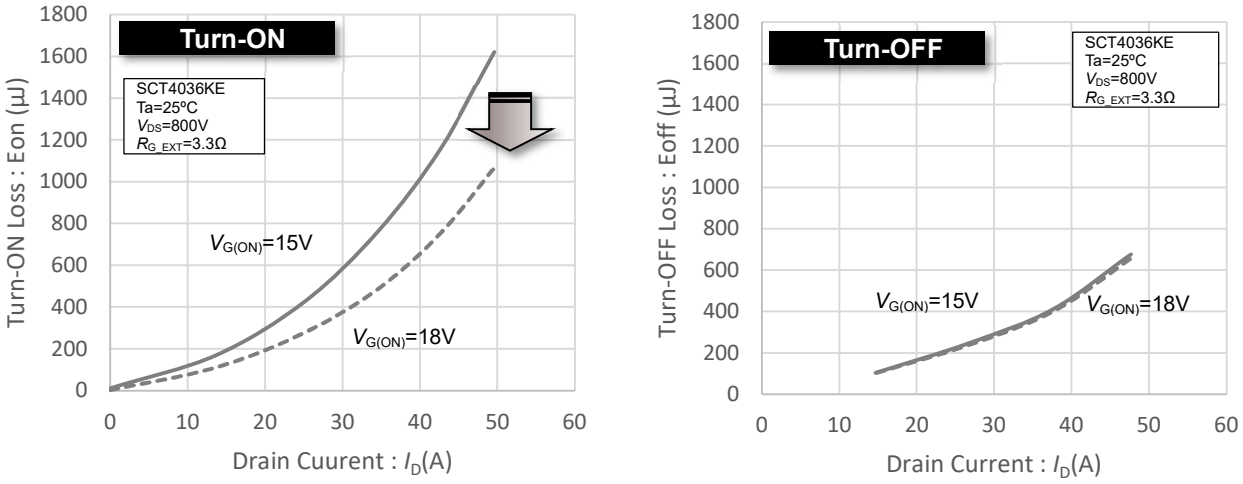


Figure 2-15. Comparison of recovery characteristics of body diodes

2.11 Dependence of switching loss on gate voltage

Figure 2-16 shows the difference in the switching loss due to the gate drive voltage. The switching loss when the device is turned ON (E_{ON}) decreases as the driving supply voltage $V_{G(ON)}$ increases. E_{ON} at 18 V is reduced by approximately 1.6 times compared with 15 V when I_D = 50 A. This is because gate current $I_{G(ON)}$ increases as the potential difference between $V_{G(ON)}$ and the plateau voltage increases, accelerating the discharge of C_{rss}, i.e., the fall speed of drain voltage V_{DS} (Figure 2-17 (a)). The plateau voltage is the gate voltage value at which the charge/discharge of the Miller capacitance begins during switching.

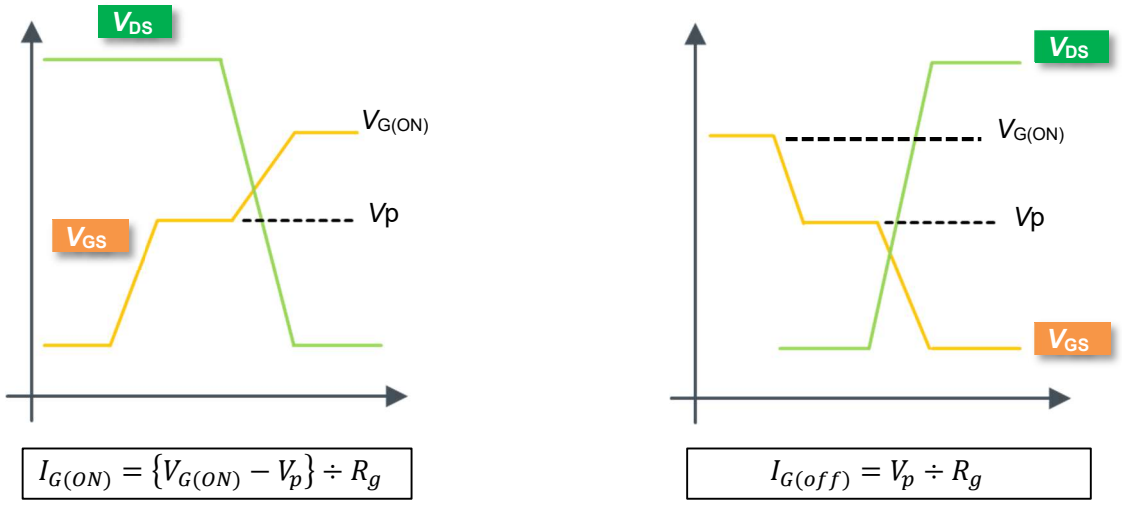
In contrast, the switching loss when the device is turned OFF (Eoff) shows little variation with $V_{G(ON)}$. When the device is turned OFF, since the gate current that charges Crss ($I_{G(off)}$) is determined by the potential difference between plateau voltage V_p and the gate OFF voltage (0 V in this case), Eoff is not affected by $V_{G(ON)}$ (see Figure 2-17 (b): Clearly, $V_{G(ON)}$ is not included in the expression of $I_{G(off)}$).



(a) Turn-on loss: Eon

(b) Turn-off loss: Eoff

Figure 2-16. $V_{G(ON)}$ dependence of switching loss



(a) During turn-on

(b) During turn-off

Figure 2-17. Gate current I_G during turn-on/off

2.12 Short-circuit rating

For the 4th Gen SiC MOSFETs, by employing a unique device structure, the inherent trade-off between RonA and the short-circuit withstand time is resolved, and low RonA and high short-circuit rating are simultaneously achieved (Figure 2-18). The short-circuit withstand time is generally shortened if RonA is decreased, because the saturation current increases. However, the peak current when a short-circuit occurs is suppressed in the 4th Gen SiC MOSFETs by decreasing the saturation current of drain-source current I_D compared with the 3rd Gen SiC MOSFETs. Therefore, the trade-off between RonA and the short-circuit withstand time is successfully resolved to secure the short-circuit withstand time (Figure 2-19). (The short-circuit ratings shown in the figure are measured values under a certain condition. Note that these numerical values are not guaranteed.)

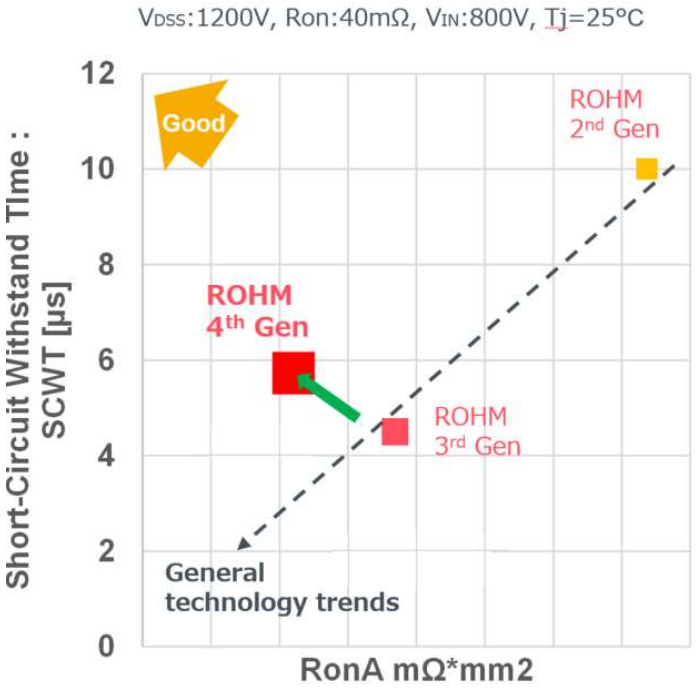


Figure 2-18. RonA vs. short-circuit withstand time

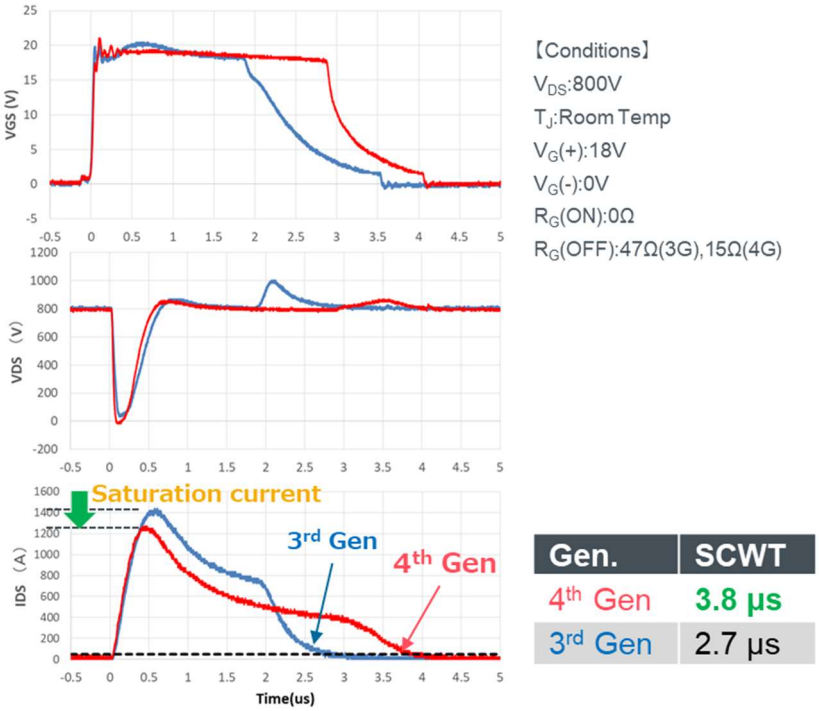


Figure 2-19 Comparison of saturation current (4th Gen vs. 3rd Gen)

• 3. Gate drive

The slew rate (dv/dt) of the 4th Gen SiC MOSFETs when being driven is significantly increased compared with the 3rd Gen SiC MOSFETs. On one hand, the characteristics are expected to decrease the switching loss and improve the efficiency. On the other hand, the occurrence of ringing or surge may be induced. Therefore, designing the gate drive circuits requires even more precautions and careful considerations. In this chapter, we explain the precautions for designs related to the gate drive and the recommended driving conditions among other points.

3.1 Gate driver IC for SiC MOSFET

When selecting a gate driver IC for the SiC MOSFET, the following points must be particularly considered.

- Driving voltage (e.g., the maximum rating)
- Driving ability (e.g., output peak current and switching frequency)
- Propagation delay time (e.g., between the primary and secondary sides)
- Protection function (e.g., Miller clamp, DESAT, OCP, and UVLO)
- Tolerance to the common mode transient voltage (CMTI: Common Mode Transient Immunity)

In addition, driver ICs are roughly categorized into two types: single function (Simple) and multifunction (Complex) types. The single function type features only the gate drive function with drive signals, and is produced as small packages including SOP-8 and SSOP-10. In contrast, the multifunction type supports negative bias and features various protection functions, the temperature monitoring function, isolated power supply, and so on. Many of these products are available as a large package of SOP-20 and greater.

Many products that provide various required functions are included in the lineup. Please visit ROHM's website (https://www.rohm.com/products/power-management/gate-drivers) or contact our sales representative for more details.

3.2 Recommended gate voltage ($V_{G(on)}$)

The 4th Gen SiC MOSFETs support not only driving with 18 V, but also driving with 15 V, which is not available for the 3rd Gen products. Therefore, previous circuits for Si-based devices can be transferred. Furthermore, although the devices are designed to be optimized when driven with 18 V, an efficiency equivalent to the optimized value with 18 V can be achieved depending on the conditions. Figure.3-1 shows the results of comparison of the efficiencies when $V_{G(ON)}$ is set to 15 V or 18 V under the described conditions. Although a slight difference is observed under a heavy load, the efficiencies are nearly equivalent. Therefore, it is easy to replace the Si MOSFET driven with 15 V.

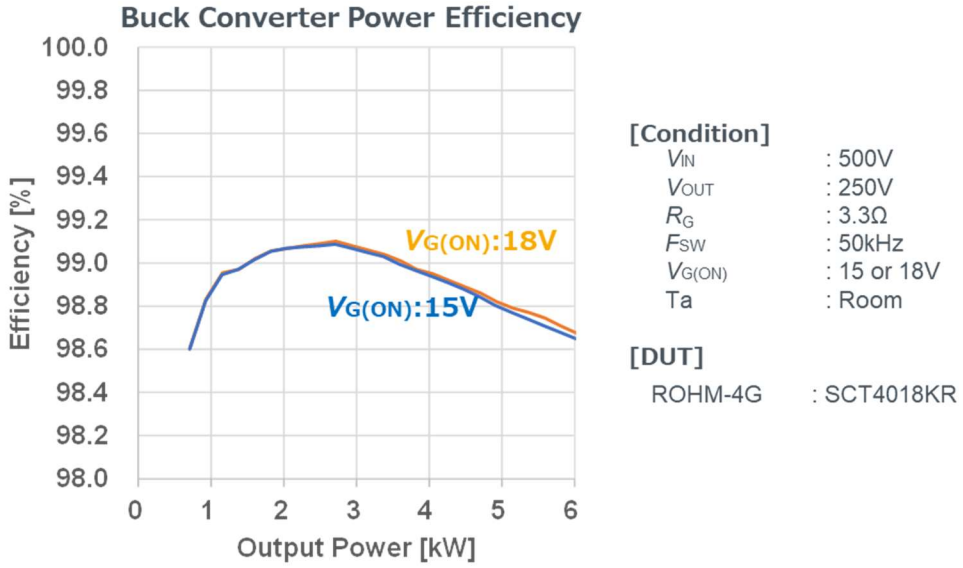


Figure 3-1. Comparison of efficiencies with varied voltage $V_{G(ON)}$ (buck converter operation)

In addition, the recommended drive voltage during turn-off is 0 V for the 4th Gen SiC MOSFETs. For general MOSFET, the gate-source voltage can be applied up to negative bias during turn-off as a countermeasure against the self-turn-on. The negative bias drive is even recommended for some products. However, for the 4th Gen SiC MOSFETs, the threshold voltage (V_{th}) is designed to be high in order to suppress the occurrence of the self-turn-on, eliminating the need for the application of negative bias. (Figure.3-2)

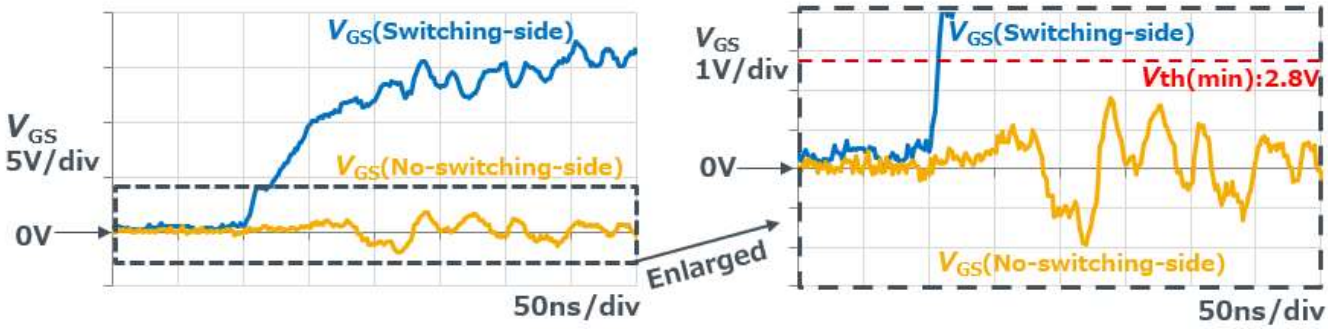


Figure 3-2. Waveforms when switching is turned ON

Since the gate voltage rating of ROHM's SiC MOSFET varies for each generation, comparisons are listed in Table 3-1. For the gate voltage rating of the SiC MOSFET, refer to Chapter 4 "Reliability of the 4th Gen SiC MOSFETs".

Table 3-1. Comparison of gate-source voltage

Parameter		3rd Generation SCT3xxxx	4 th Generation SCT4xxxx
Gate-Source Voltage		-4 V ~ +22 V	-4 V ~ +21 V
Gate-Source Surge Voltage		-4 V ~ +26 V	-4 V ~ +23 V
Recommended Drive voltage	Positive	+18 V ~ +20 V	+15 V ~ +18 V
	Negative	0 V	0 V

3.3 Selection of external gate resistance (R_{G_EXT})

One of the important factors determining the switching performance of the MOSFET is selection of the external gate resistance (R_{G_EXT}). The switching speed depends on the sum of the external gate resistance (R_{G_EXT}) and internal gate resistance (R_{G_INT}) of the device. The smaller the sum, the faster the switching speed. As described in Section 2.8, the internal gate resistance of the 4th Gen SiC MOSFETs is significantly reduced compared with the 3rd Gen SiC MOSFETs. Therefore, if the 3rd Gen SiC MOSFETs is replaced with the 4th Gen SiC MOSFETs without changing the external gate resistance, the switching speed is increased and the switching loss can be reduced (refer to Section 2.6 “Turn-on/turn-off characteristics”). However, if the switching speed is increased, the surge voltage between the gate and the source tends to increase.

Figure 3-3 shows the waveforms of V_{GS} on the no-switching side and the waveforms of V_{DS} and I_D on the switching side when the 4th Gen SiC MOSFETs “SCT4062KR” (1,200 V, $R_{DS(on)}$ = 62mΩ) is switched. The figure indicates that the smaller the gate resistance value, the faster the switching speed for V_{DS} and I_D. However, it also shows that the surge of V_{GS} on the no-switching side is increased.

Based on these factors, it is important to repeat evaluations to select a value of the external gate resistance that satisfies the required operation efficiency by suppressing the switching loss while preventing the surge voltage from reaching the rated value for the device.

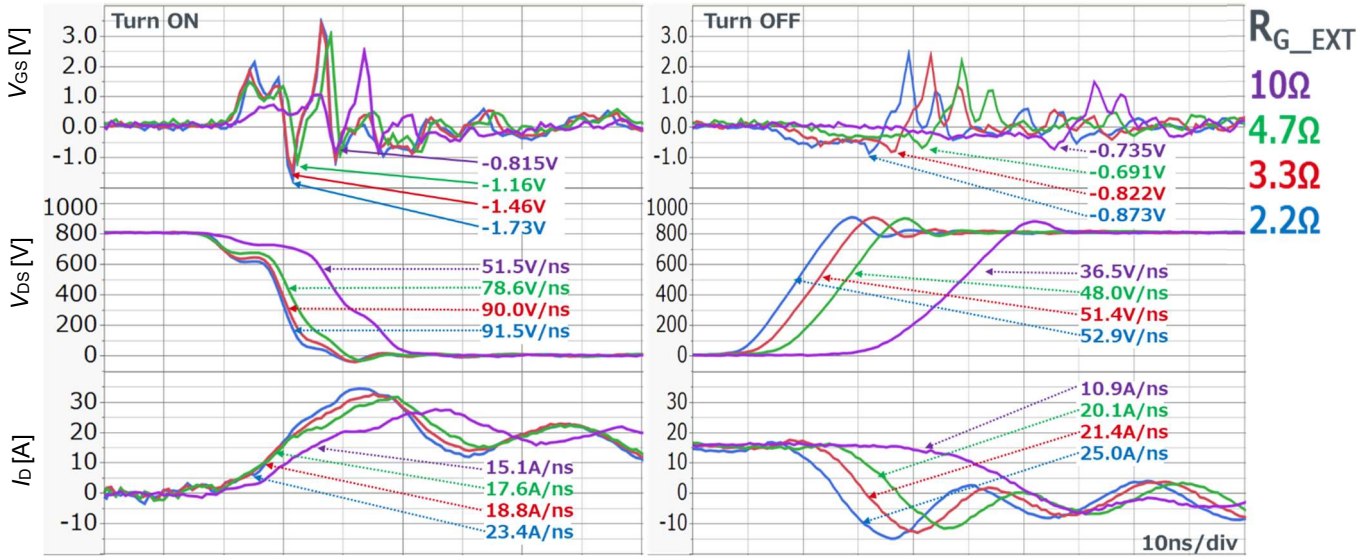
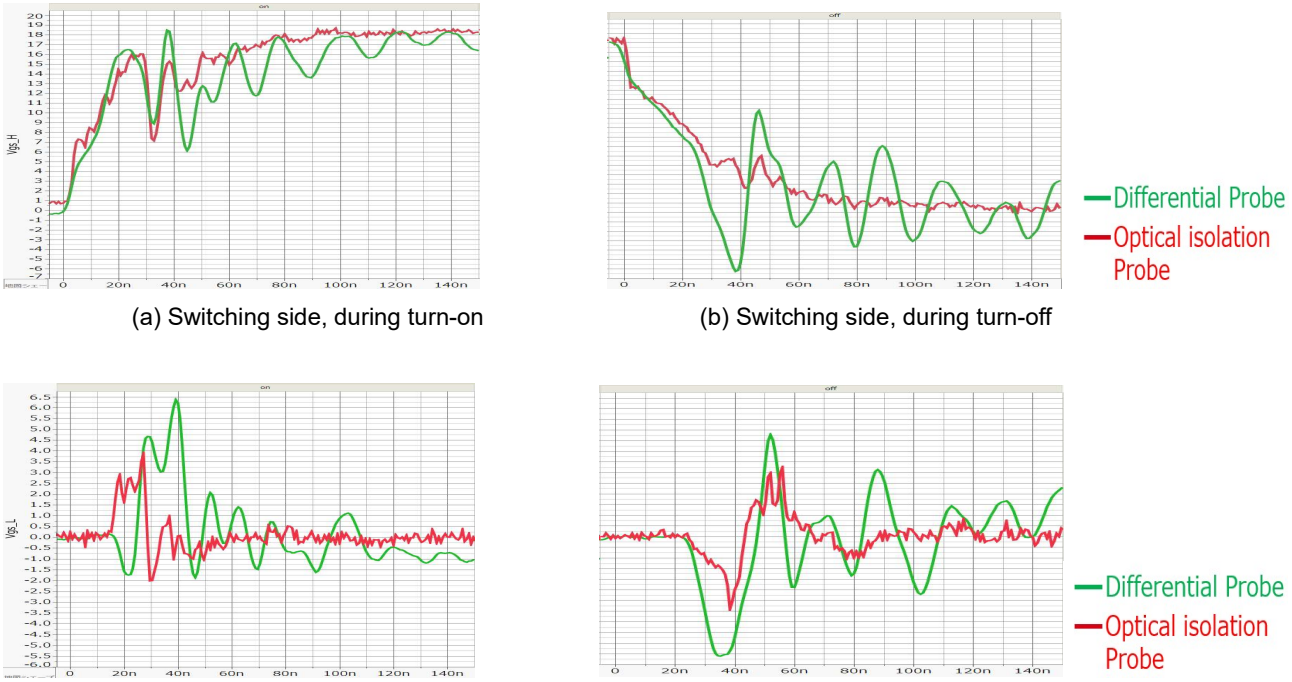


Figure 3-3. R_{G_EXT} dependence of V_{GS} waveforms when switching is turned ON/OFF (SCT4062KR)

3.3.1 Precautions for measuring the V_{GS} surge

The slew rate during switching of the SiC MOSFET is significantly increased compared with the Si MOSFET. Therefore, it is difficult to acquire accurate waveforms with measurements using a conventional passive or differential probe due to noise and other problems caused by the probe. Therefore, to measure fast switching waveforms, such as those in the SiC MOSFET, it is recommended to use an optical isolation probe, which can cut the effect of noise. Figure 3-4 shows how the double pulse test is conducted using an optical isolation probe. For details of the test and the board used, refer to “5. Evaluation board for discrete devices”.

Figure 3-5 shows the results of comparison between acquisitions of the switching waveforms using a differential probe and an optical isolation probe under the same condition. It can be seen that large surges occur in the waveforms measured with the differential probe.



(a) Switching side, during turn-on

(b) Switching side, during turn-off

(c) No-switching side, during turn-on

(d) No-switching side, during turn-off

Figure 3-5. V_{GS} waveforms when switching is turned ON/OFF (SCT4036KR)

For details on the precautions for measuring SiC devices, refer to Application Note “Precautions during gate-source voltage measurement”*6 as well.

3.3.2 Countermeasures against V_{DS} surges

Although the SiC MOSFET features the high-speed switching, a higher surge voltage occurs between the drain and source. Therefore, it is necessary to select R_{G_EXT} so that the drain-source voltage is contained within the voltage rating like the V_{GS} surge voltage. Adding a surge absorption circuit, such as a snubber circuit, is also an effective countermeasure. Figure 3-6 shows an example of the snubber circuit.

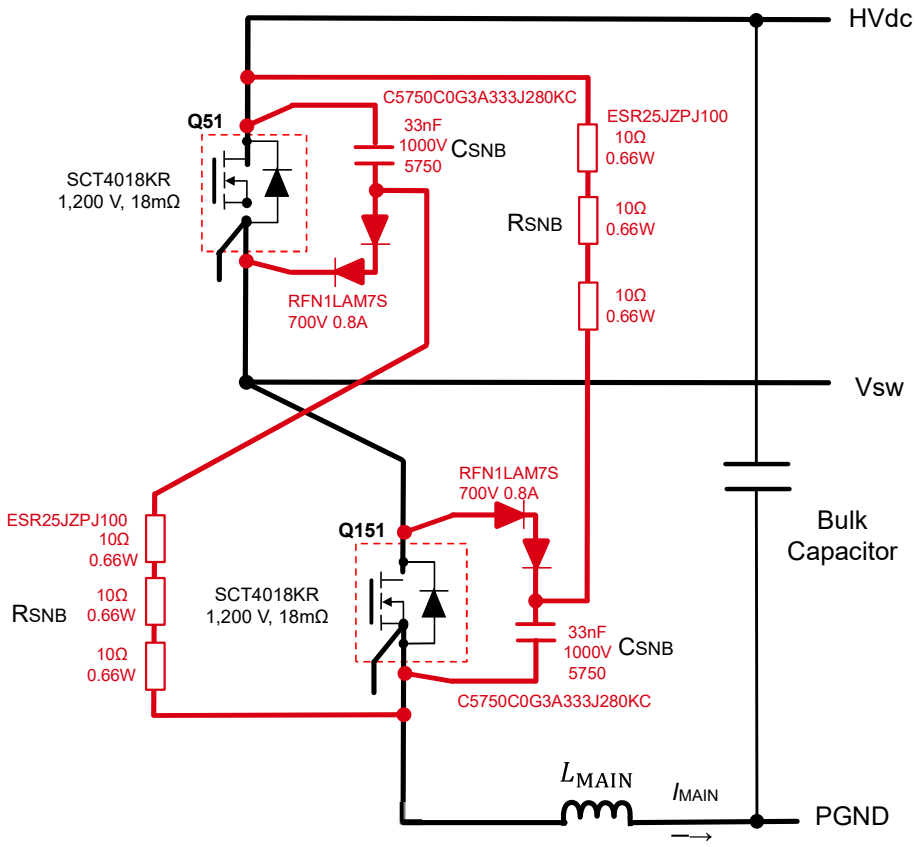


Figure 3-6. Example of snubber circuit (SCT4018KR)

The non-discharge snubber circuit is ideal for high-frequency switching circuits because only the surge exceeding the high-voltage input HVdc is consumed by the resistors in the snubber circuit. However, since the pattern layout is complicated, it should be used on boards with four or more layers.

The power consumed by the resistor in the snubber circuit (P_{SNB}) is entirely consumed by the resistor in the snubber circuit (R_{SNB}). Therefore, to set R_{SNB}, derive P_{SNB} from Equation (1) first.

$$P_{SNB} = \frac{L_{MAIN} \times {I_{MAIN}}^2 \times f_{SW}}{2} \quad [W] \cdots (1)$$

In this equation, L_{MAIN} is the wiring inductance of the main circuit, which includes the equivalent series inductance of the bulk capacitor. I_{MAIN} represents the drain current in the MOSFET during turn-off, and f_{SW} represents the switching frequency to drive the SiC MOSFET.

The capacitance of the snubber capacitor (C_{SNB}) is calculated from the energy stored in the inductance with Equation (2) below.

$$C_{SNB} = \frac{L_{MAIN} \times {I_{MAIN}}^2}{{V_{SURGE}}^2 - {V_{HVdc}}^2} \quad [F] \cdots (2)$$

Where V_{HVdc} is the high-voltage power supply and V_{SURGE} is the maximum surge voltage. Furthermore, the resistance of R_{SNB} can be calculated with Equation (3) below.

$$R_{SNB} < \frac{-1}{C_{SNB} \times \ln[(V_{SURGE} - V_{SNB})/(V_{SURGE})]} \times \frac{1}{f_{sw}} \quad [\Omega] \cdots \quad (3)$$

Correctly setting the R_{SNB} value maximizes the surge absorption effect by discharging all the energy absorbed by C_{SNB} during one cycle of the SiC MOSFET.

Figure 3-7 shows the verification results of the snubber circuit of the SCT4018KR from the double-pulse test. During turn-on, there is almost no difference between with and without the snubber circuit, but during turn-off, the V_{DS} turn-off surge is reduced from 1,206 V to 1,070 V. On the other hand, there is little effect on the switching speed.

Therefore, the V_{DS} turn-off surge can be suppressed by mounting the snubber circuit. In case the V_{DS} turn-off surge causes a problem, it is recommended to consider employing a snubber circuit from the circuit design phase.

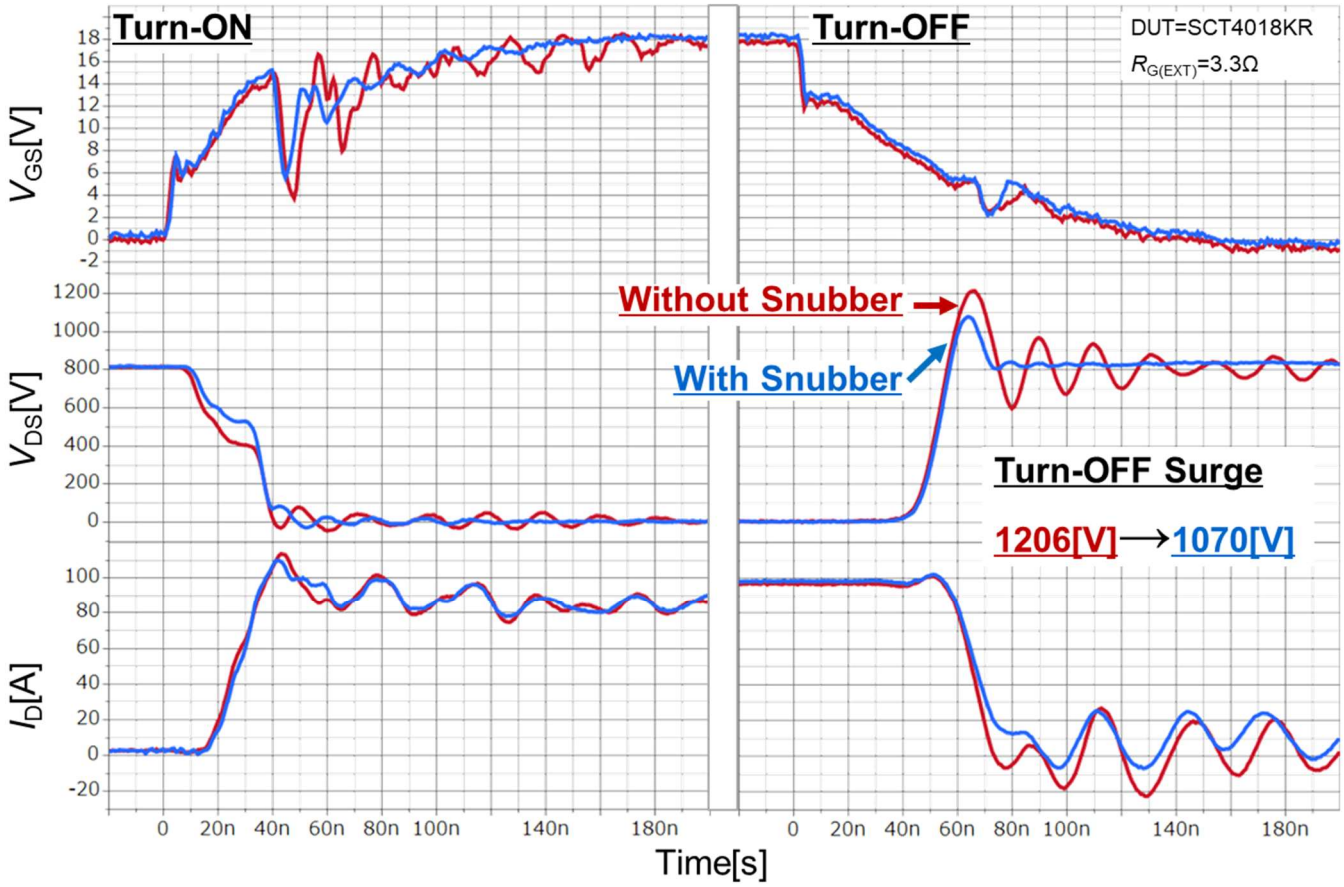


Figure 3-7. Effect of snubber circuit（SCT4018KR）

For details of how to design snubber circuits, refer to Application Note "Snubber circuit design methods"*4.

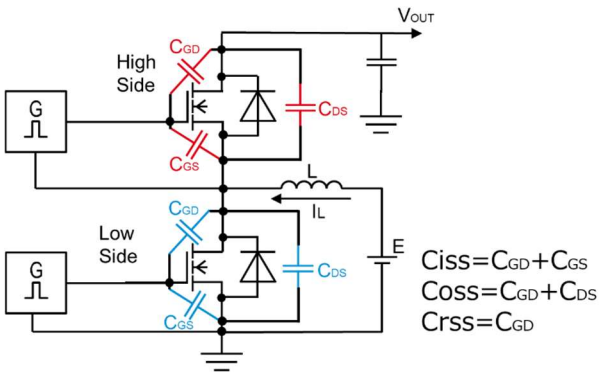
3.4 Dead time (t_{DT}) design

If the SiC MOSFET is used in a circuit with the bridge structure, dead times are usually provided so that the SiC MOSFET on the high side (HS) and the low side (LS) will not be turned ON simultaneously. Figure 3-8 (a) shows a case example of the dead time control in a boost circuit. The low-side and high-side SiC MOSFET operate for switching and synchronous rectification, respectively. As shown in (b), dead times are provided before LS is turned ON and after LS is turned OFF to prevent HS and LS from turning ON simultaneously. During the dead times, the current of inductor *L* flows through the body diode of the SiC MOSFET. Since forward voltage V_F of the body diode of the SiC MOSFET is higher than that of the Si devices, it is considered desirable to shorten the dead times as much as possible.

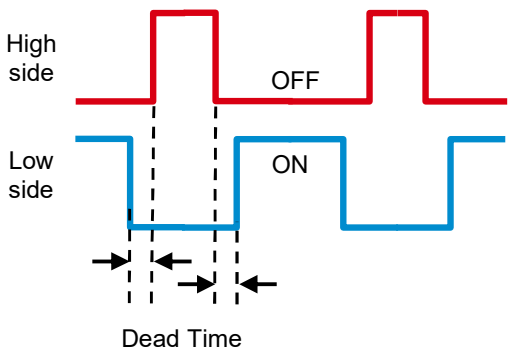
However, if the current of inductor *L* during turn-off ($I_{L(OFF)}$) decreases, the charge/discharge currents to the output capacitances (C_{oss}) of the high-side and low-side SiC MOSFET also decrease. As a result, the charge/discharge of C_{oss}, i.e., the variation in V_{DS}, cannot be completed within the dead times. In this case, the switching loss, which should not occur originally, is generated in the synchronous rectification SiC MOSFET, and issues such as reduced efficiency and increased heat generation occur. Therefore, it is necessary to estimate the minimum value of the dead times according to the operation condition of $I_{L(OFF)}$.

The minimum dead time shown in Equation (3) is calculated with a constant C_{oss} for the sake of simplification. However, actual C_{oss} varies with drain-source voltage V_{DS}. In many cases, C_{oss} described in the data sheet is generally a representative value at a certain V_{DS} and not necessarily the most suitable value for calculating the dead times. By using the V_{DS}-C characteristics shown in Figure 3-9 and calculating C_{oss} with V_{DS} <1 V where C_{oss} is maximized, the dead times can be designed with a margin (shaded area). Actual electric charge required for the charge/discharge corresponds to the colored area in the figure. Therefore, t_{DT} can also be calculated more accurately by using this area part for the numerator in Equation (3). The capacitance graphs such as Figure 3-9 are presented in the data sheets of the SiC MOSFET.

$$t_{DT} > \frac{(C_{OSS\_HS}+C_{OSS\_LS})\times V_{OUT}}{I_{L(off)}} \quad (3)$$



(a) Boost circuit



(b) PWM pulse timing

Figure 3-8. Dead time control in boost circuit

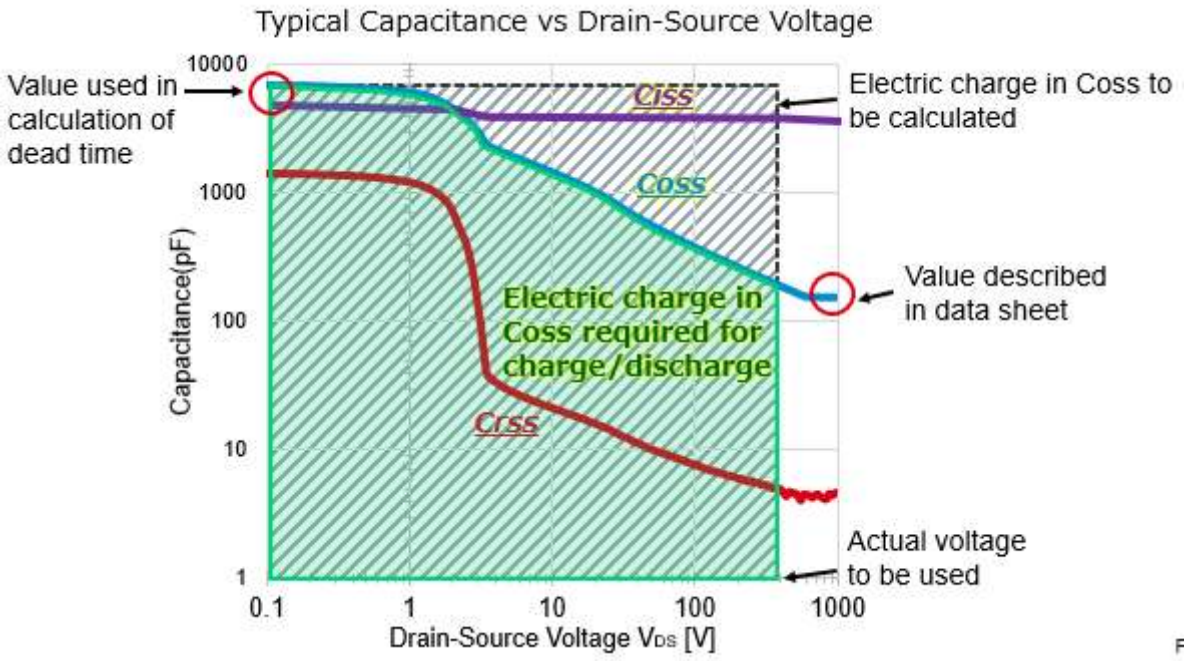


Figure 3-9. V_{DS} dependence of parasitic capacitance (SCT4018KR)

3.5 Countermeasures against self-turn-on

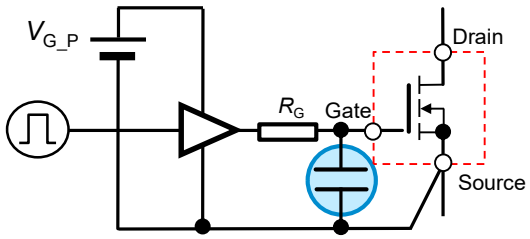
If MOSFET are used in bridge structures, such as inverters and full bridge circuits, the MOSFET on either or both of the upper and lower arms are supposed to be simultaneously turned OFF. However, due to variation in V_{DS} or I_D on the non-switching side (reflux side) responding to the operation of the switching side MOSFET, they can be accidentally turned ON. This is referred to as the self-turn-on. When this phenomenon occurs, not only is the efficiency reduced, but the MOSFET may also be damaged in the worst case.

A negative bias is generally applied to the voltage while the device is turned OFF as a countermeasure against the self-turn-on. The negative bias drive is even recommended for many products.

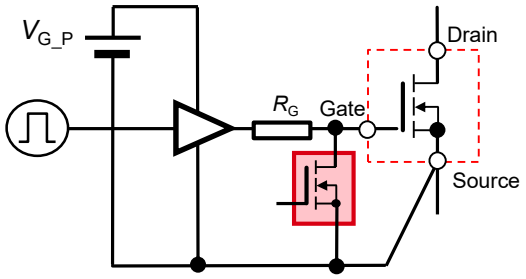
Since the threshold voltage (V_{th}) is designed to be high for the 4th Gen SiC MOSFETs, the occurrence of the self-turn-on is suppressed. Therefore, the negative bias drive is not required. In the evaluations using ROHM's evaluation boards (P04SCT4018KE-EVK-001 and P05SCT4018KR-EVK-001) described in Chapter 5, no occurrence of the self-turn-on was observed.

However, when a board is designed by customers, the self-turn-on may occur due to the wiring inductance and other factors. In such cases, countermeasures against the self-turn-on must be built into the circuit.

Figure 3-10 shows examples of circuits used for countermeasures. In (a), by connecting a capacitor of 1 nF to 5 nF between the gate and source of the MOSFET, an instantaneous rise of the gate voltage is prevented. In (b), by using an active Miller clamp MOSFET that is turned ON below a certain value of the gate-source voltage, a rise of the gate-source voltage is prevented. In these circuits used for countermeasures, since the effects are diminished if the parasitic inductance exists, it is important to install the parts for countermeasures as proximate as possible to the gate and source terminals. It is also recommended to select parts in a small package with a small parasitic inductance.



(a) Capacitor connected between gate and source



(b) Active Miller clamp MOSFET

Figure 3-10. Examples of countermeasures against self-turn-on in bridge structure

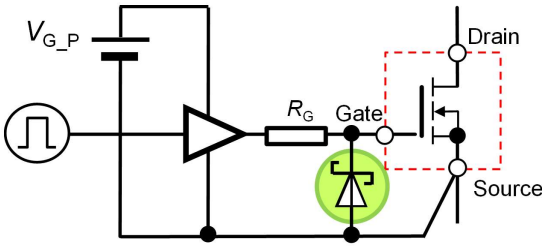
However, each system used as a countermeasure against the self-turn-on has advantages and disadvantages, and may not be applicable depending on the functions of the gate driver IC to be used. Please understand the generation mechanism of self-turn-on correctly and make a selection.

The generation mechanism of self-turn-on is detailed in Application Note "Gate-source voltage behaviour in a bridge configuration"*2. In addition, various circuits for countermeasures are presented in Application Note "Gate-Source Voltage Surge Suppression Methods"*3. Please refer to this application note as well.

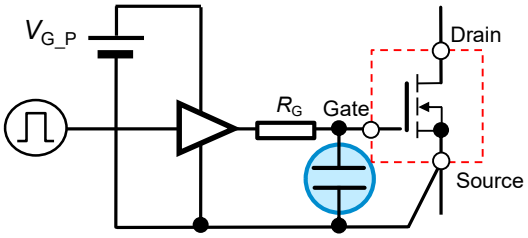
3.6 Countermeasures against negative surge

As explained in Section 3.5, the gate voltage rating of the SiC MOSFET is very narrow. In particular, the margin for the voltage during actual use is only a few V regarding the negative bias. Therefore, it is very important to include countermeasures against the gate negative surge from the circuit design phase.

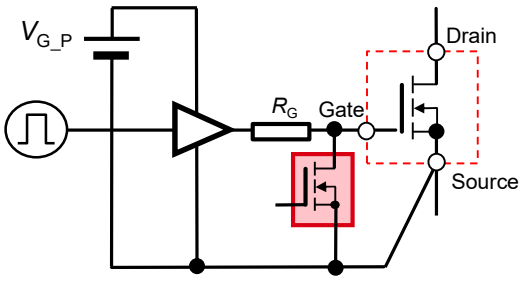
Figure 3-11 shows circuits used as countermeasures against the negative surge. In (a), a diode to clamp the negative surge is connected between the gate and the source. In (b), by connecting a capacitor of 1 nF to 5 nF between the gate and source of the MOSFET, an instantaneous drop of the gate voltage is prevented. In (c), by using an active Miller clamp MOSFET that is turned ON below a certain value of the gate-source voltage, a drop of the gate-source voltage is prevented. The countermeasures in (b) and (c) are identical to the countermeasures against the self-turn-on described in Section 3.5 and these countermeasures can be shared. In addition, like the countermeasures against the self-turn-on, it is important to install the parts for countermeasures proximate to the gate and source terminals and select parts with the smallest parasitic inductance possible.



(a) SBD connected between gate and source



(b) Capacitor connected between gate and source



(c) Active Miller clamp MOSFET

Figure 3-11. Countermeasures against negative surge in the bridge sector

However, the negative surge is not necessarily caused by a single factor, but caused by multiple factors closely connected with the timing of variations in V_{DS} and I_D. Effective countermeasures depend on the timing of occurrence of the negative surge. Therefore, it is necessary at first to accurately understand the factors causing the negative surge. It is important to take the best countermeasures according to the circumstances, such as the presence or absence of the negative bias and the board layout conditions, based on this understanding.

The generation mechanism of negative surge is detailed in Application Note "Gate-source voltage behaviour in a bridge configuration"*2. In addition, various circuits used as countermeasures are presented in Application Note "Gate-Source Voltage Surge Suppression Methods"*3. Please refer to this application note as well.

3.7 Recommended layout

We have explained the following functions of the gate drive circuits:

• Gate driving power supply (Section 3.2)

• Gate resistance (adjusting the switching speed, Section 3.3)

• Gate surge protection (MOSFET gate protection, Section 3.6)

All of these required circuit parts must be mounted on the printed board. Ideally, all functions should be mounted near the MOSFET. However, it is necessary to set priorities on the board layout.

In addition, the amplitude of the surge voltage occurring at the gate depends on the characteristics and circuit topology of the device to be used. Therefore, the priorities of countermeasures also depends on the device to be used. When considering the layout of a circuit around the MOSFET, careful examination is required regarding the pattern inductance of which function should be reduced.

To categorize the circuit topologies, they can be distinguished based on the MOSFET structures and the switching systems. Namely, they can be roughly distinguished into the structure using a single MOSFET (single) and the structure using the upper and the lower MOSFET connected in series (half bridge), and further categorized into the hard switching system (hard switching) and the soft switching system (soft switching) as the switching system of the MOSFET. In the half bridge structure, the non-switching side is affected by the operation on the switching side. In contrast, since a single MOSFET is used in the single structure, it is sufficient to consider its own switching operation only.

In addition, since the switching characteristics and the gate voltage rating vary with the device generations, pay attention to the different protection functions required for each generation.

Table 3-2 shows the required functions for each circuit structure. By determining the layout priorities of the parts for countermeasures in the following order, it is important to achieve operations within the rating and a high efficiency simultaneously.

Table 3-2. Required functions in gate drive circuit

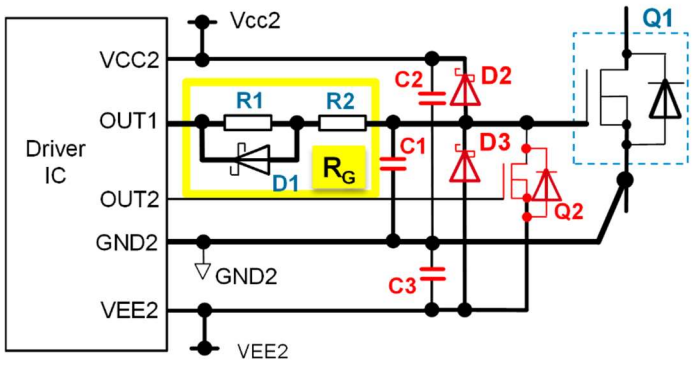
Topology		Protection function required
Single End	Hard Switching Soft Switching	1) SBD connected between gate and source 2) Gate resistance
Half Bridge	Hard Switching	1) Active Miller clamp MOSFET 2) Negative surge clamp SBD 3) Capacitor connected between gate and source 4) Gate resistance
	Soft Switching	1) SBD connected between gate and source 2) Capacitor connected between gate and source 3) Gate resistance

Figure 3-12 shows a layout example for the half bridge evaluation board for the SiC MOSFET (P05SCT4018KR-EVK-001): (a) drive circuit diagram, (b) picture of the mounted board, and (c) and (d) layout of the board pattern.

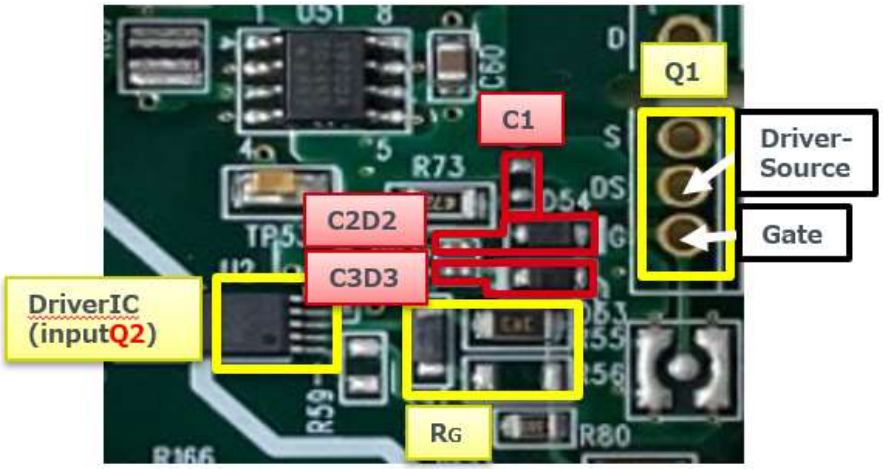
Since this board is used to evaluate the 4th Gen SiC MOSFETs with the hard switching operation, the countermeasures against gate surges are the most important. The MOSFET (Q2) must be placed proximate to the SiC MOSFET as much as possible. However, since the gate driver IC (BM61M41RFV-C) being used in the board shown in Figure 3-12 (b) has a built-in active clamp MOSFET, the diode for absorbing the negative surge (D3) and its bypass capacitor (C3) are placed proximate to the gate driver IC. Next, the diode for absorbing the positive surge (D2) and its bypass capacitor (C2) are laid out. Since the positive surge is generated due to the inductance caused by the pattern length from the driver IC to the MOSFET, whether or

not the mounting is possible is judged according to the layout situation. Finally, the capacitor used as a countermeasure against self-turn-on (C1) is placed between the gate and the source.

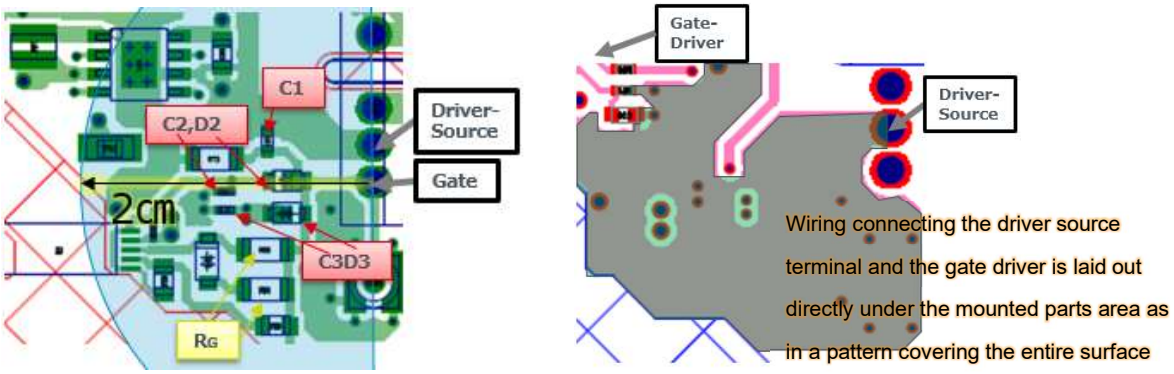
The effect of the surge absorption parts is diminished as the distance from the MOSFET increases. Therefore, it is recommended to place the parts within 2 cm from the MOSFET as shown in (c). In addition, it is important to lay out the return line from the driver source terminal to the gate driver IC directly under all the driver circuit parts, as in pattern (d) covering the entire surface, so that the effect of external noise on the drive signal and the surge protection circuit can be reduced as much as possible.



(a) Example of gate surge protection circuit



(b) Example of gate surge protection circuit mounted on PCB (P04SCT4018KR-EVK-001)



(c) Parts mounted surface (d) Back surface

Figure 3-12. Layout example of gate surge protection circuit (P05SCT4018KR-EVK-001)

• 4. Reliability of the 4th Gen SiC MOSFETs

Table 4-1 shows the result of the reliability test. (Consumer and industrial applications)

Table 4-1. Items and result of reliability test for through-hole type (TO-247N/TO-247-4L)

Product	MOSFET	Package	Through Hole Devices	Type	SCT4*** 6inch wafer

1. Life Test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
High Temperature Reverse Bias	$T_a = T_{jmax}$, $V_{DS} = V_{DSmax}$ JEITA ED-4701/100A-101A	1000 h	22	0
High Temperature Gate Bias	$T_a = T_{jmax}$, $V_{GS} = V_{GSmax}$ JEITA ED-4701/100A-101A	1000 h	22	0
High Temperature Gate Bias	$T_a = T_{jmax}$, $V_{GS} = V_{GSmin}$ JEITA ED-4701/100A-101A	1000 h	22	0
Temperature humidity bias	T_a= 85℃, RH = 85%, V_{DS} = 100V JEITA ED-4701/100A-102A	1000 h	22	0
Temperature cycle	T_a = -55℃ (30 min) ~ T_a = 150℃ (30 min) JEITA ED-4701/100A-105A	100 cycles	22	0
Pressure cooker	T_a = 121℃, 203kPa [2 atm], RH = 100% JESD22-A102C	48 h	22	0
High Temperature storage	T_a = 175℃ JEITA ED-4701/200A-201A	1000 h	22	0
Low Temperature storage	T_a = -55℃ JEITA ED-4701/200A-202A	1000 h	22	0

2. Stress Test

Test Item	Test Method/ Standard	Test Condition	Sample Size n [pcs]	Failure(s) Pn [pcs]
Resistance to solder heat 1	Dipping leads into solder bath at 260 ±5℃. JEITA ED-4701/301-302A	10 s	22	0
Resistance to solder heat 2	Dipping leads into solder bath at 350 ±10℃. JEITA ED-4701/301-302A	3.5 s	22	0
Solderability	Dipping into solder bath at 245 ±5℃. JEITA ED-4701/301-303A	5 s	22	0
Thermal shock	0^{+5}_{-0} (5 min) ~ 100^{+0}_{-5} (5 min) JEITA ED-4701/302-307B	100 cycle	22	0
Terminal strength (Pull)	Pull force = 20 N JEITA ED-4701/400A-401A	10 s	22	0
Terminal strength (Bending)	Bending Load = 10 N JEITA ED-4701/400A-401A	2 times	22	0

※ Failure criteria : According to the electrical characteristics specified by the specification.
Regarding solderability test, failure criteria is 95% or more area covered with solder.

※ Sample standard:[Reliability level: 90%][Failure reliability level(λ1): 10%][C=0 decision] is adopt
And the number of samples is being made 22 in accordance with single sampling inspection pla
with exponential distribution type based on MIL-STD-19500.

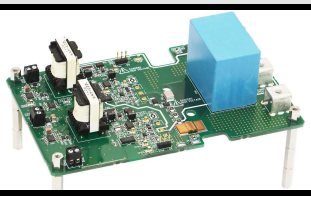
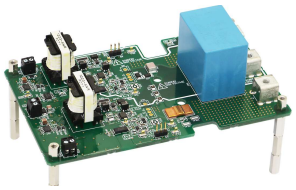
5. Evaluation board for discrete SiC MOSFET

5.1 Evaluation board for 4th Gen SiC MOSFETs (discrete)

Table 5-1 shows a list of evaluation boards released by ROHM for the 4th Gen SiC MOSFETs (discrete). The half bridge structure is employed to evaluate the switching characteristics. Evaluations of the buck and boost topologies, including the double pulse test, can be performed with the minimum number of external components. In addition, the switching speed can be adjusted and the driving voltage can be changed. The gate surge protection circuit is also installed.

For more detailed information, refer to the support page for the 4th Gen SiC MOSFETs on ROHM's website (https://www.rohm.com/products/sic-power-devices/sic-mosfet).

Table 5-1. List of evaluation boards for SiC MOSFET (discrete)

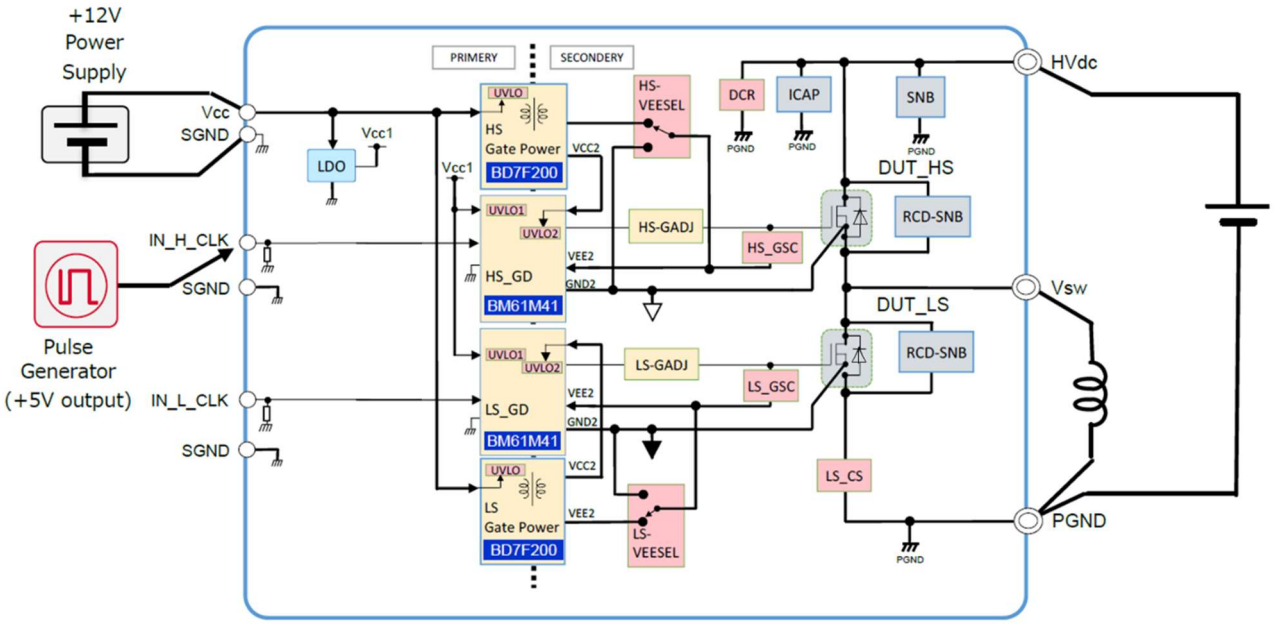
Device under evaluation	Appearance	Product name
TO-247N For 4th Gen SCT4xxxxxxxE series		P04SCT4018KE-EVK-001
TO-247-4L For 4th Gen SCT4xxxxxxxR series		P05SCT4018KR-EVK-001

This section explains an implementation example of the double pulse test using the evaluation boards, P04SCT4018KE-EVK-001 and P05SCT4018KR-EVK-001. The mounted products are SCT4036KE and SCT4036KR (1,200V, 36mΩ), respectively. Figure 5-1 shows (a) the test circuit, (b) the measurement scene, and (c) the gate drive circuit of the MOSFET.

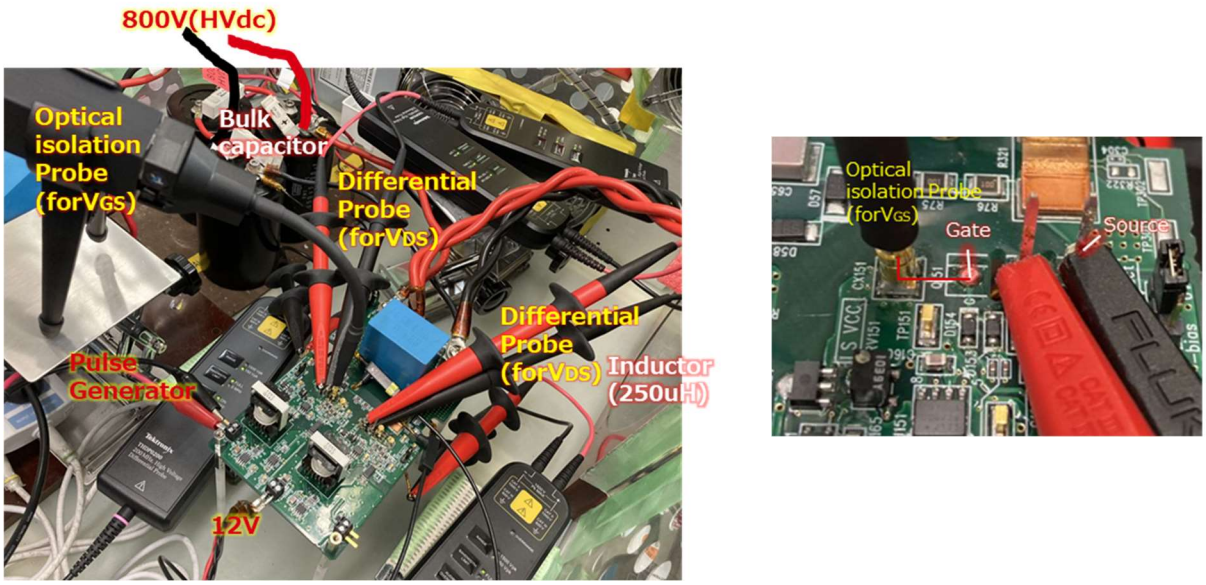
The devices required for operating the test circuits are the control power supply (12 V), pulse generator (PG), load inductor (250 µH), and high voltage load power supply (V_{HVdc}), as shown in (a). Since V_{HVdc} is located at a distance from the evaluation board, a bulk capacitor is connected in this test. A bulk capacitor is basically unnecessary because a 10 µF film capacitor is also mounted on the evaluation board. However, we recommend connecting a bulk capacitor according to the operating conditions.

The method for sensing V_{GS} during the measurement is explained in (b). The waveforms of MOSFET are usually observed with an isolation or differential probe. However, since the switching speed is increased for the SiC MOSFET, the probe is more susceptible to noise. Therefore, the connector is mounted proximate to the device and the measurement is performed with an optical isolation probe, which is not affected by the noise from the probe. In addition, the parts indicated in red dashed lines in (c) are the protection circuit to remove the surge generated between the gate and source of the MOSFET. The effect of this protection circuit is also verified.

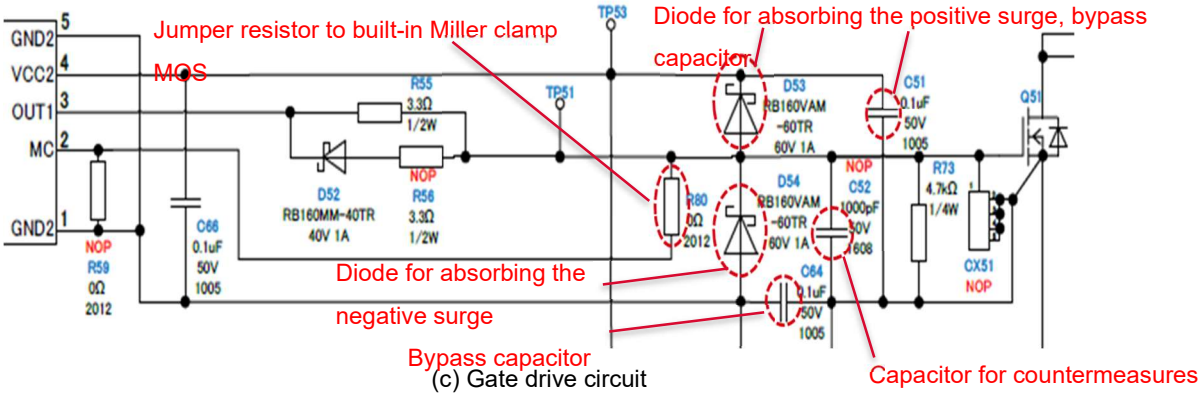
In this test, the high-side (HS) MOSFET is operated as the switching device, and a body diode is used on the low-side (LS) for commutation. The pulse width is adjusted so that V_{HVdc} is 800 V and I_D is 55 A to 60 A approximately, and the switching operation is observed when the device is turned ON and OFF. The waveforms are shown in Figures 5-2 and 5-3.



(a) Block diagram of measurement circuit (P05SCT4018KR-EVK-001)



(b) Measurement scene (P04SCT4018KE-EVK-001)

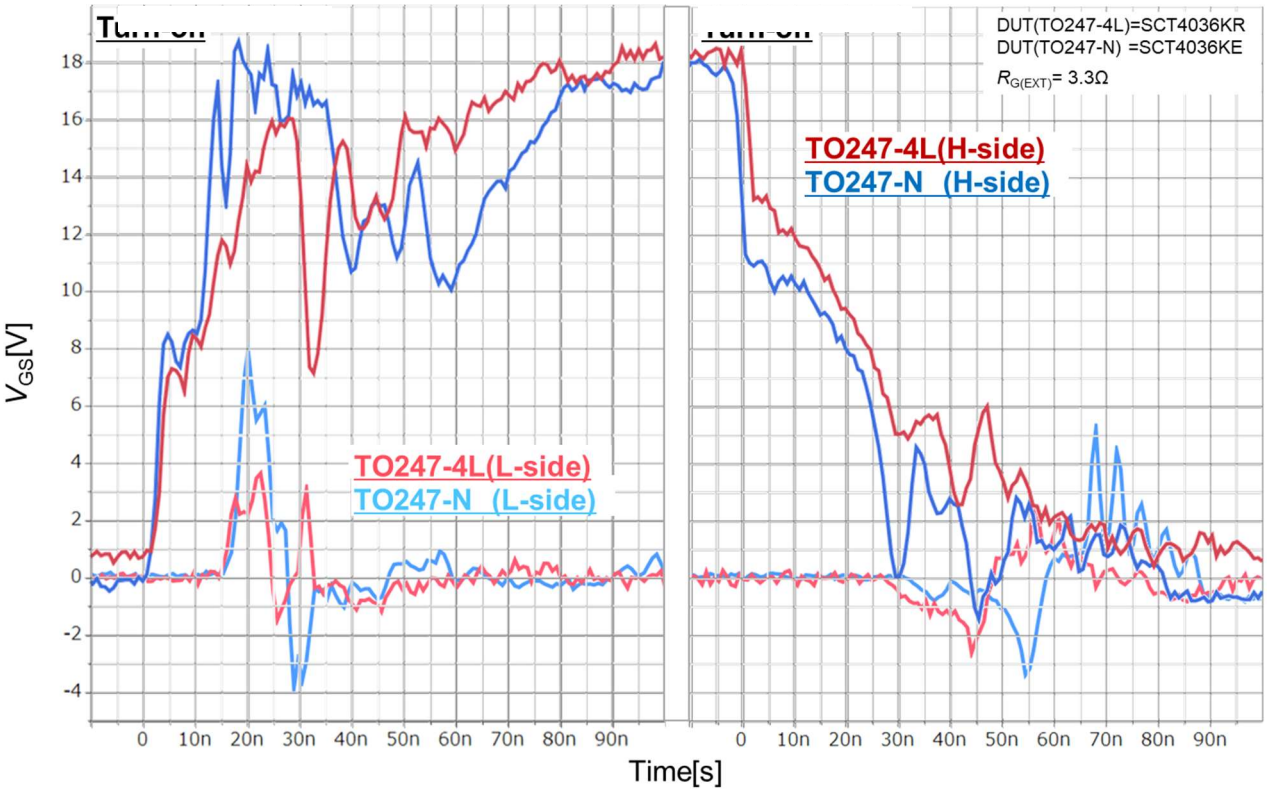


(c) Gate drive circuit

Figure 5-1. P04SCT4018KR-EVK-001 measurement circuit

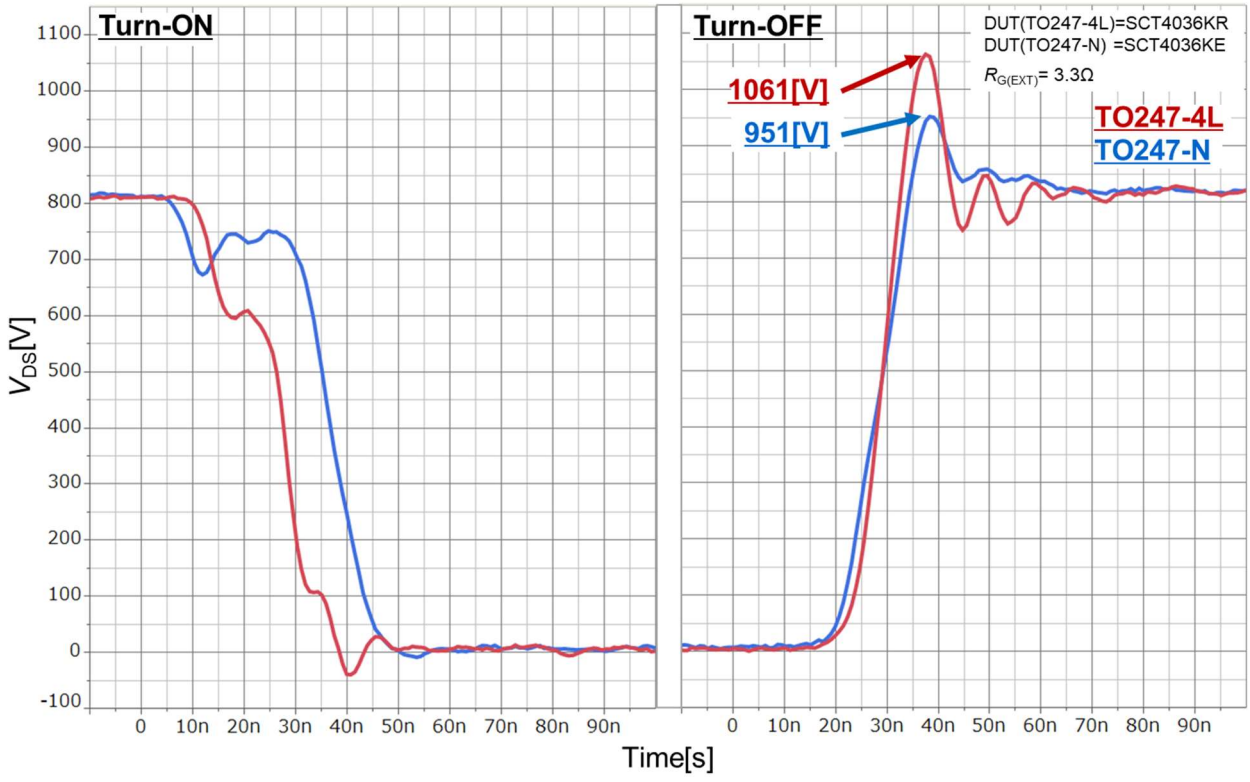
Figure 5-2 (a) shows the waveforms of V_{GS}, (b) shows the waveforms of V_{DS}, and (c) shows the waveforms of I_D, where SCT4036KE (TO-247N) and SCT4036KR (TO-247-4L) are compared. Although the V_{GS_HS} waveforms on the switching side in (a) have a nearly identical slew rate, the I_D waveforms of TO-247-4L in (c) have a much faster slew rate whether the device is turned ON or OFF. This is the effect of the driver source terminal. For more details, refer to Application Note “Improvement of Switching Loss by Driver Source Terminal” *5.

As the protection circuit shown in Figure 4-1 (c) removes the negative surge described in Section 3.6 “Countermeasures against negative surge”, the gate-source voltage on the non-switching side (LS) MOSFET (V_{GS_LS}) can satisfy the specification for the narrow gate voltage rating unique to SiC MOSFET.



(a) V_{GS} during turn-on/off (H-side, L-side)

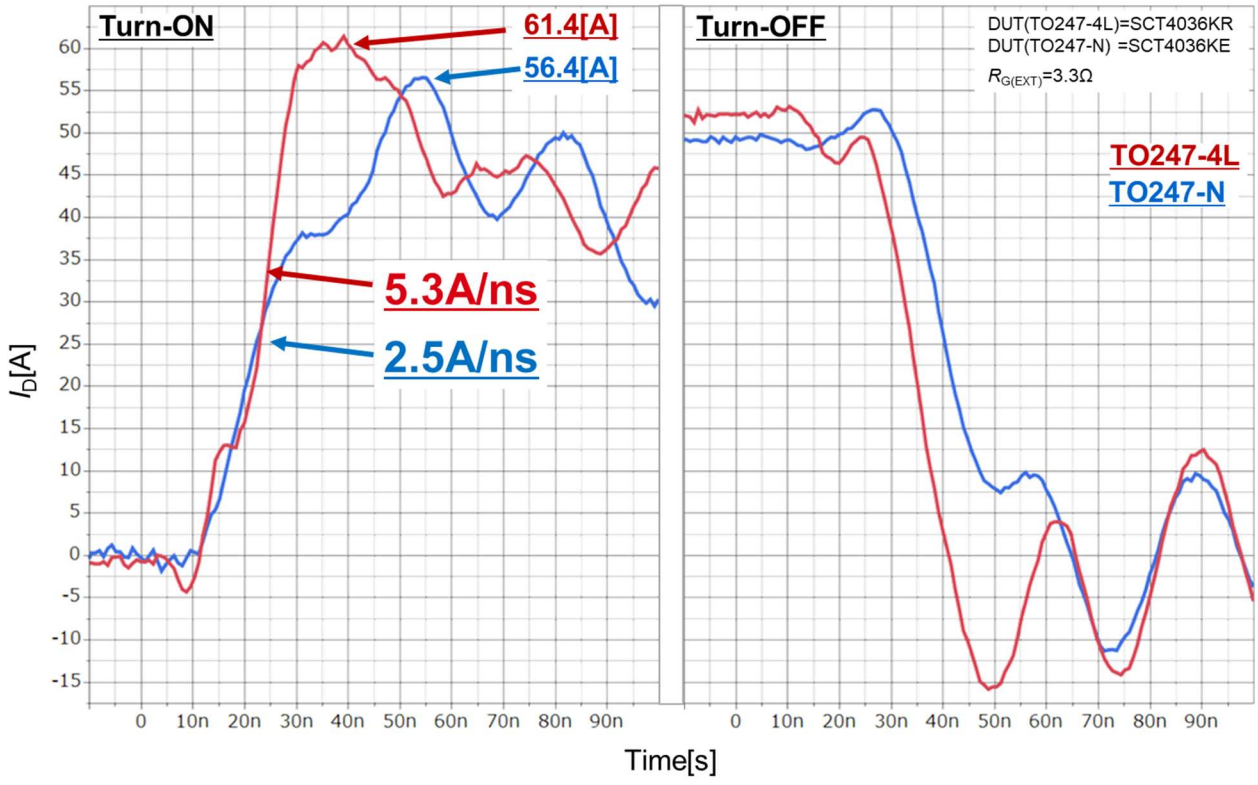
Figure 5-2 (b) shows the waveforms of V_{DS}. Although the slew rate of TO-247-4L is faster during turn-off, the value of surge is increased.



(b)

V_{DS} during turn-on/off

Figure 5-2 (c) shows the waveforms of I_D. As described in the previous page, the slew rate of TO-247-4L is faster during turn-on/off. Note that the values of surges are increased like V_{DS}.



(c) I_D during turn-on/off

Figure 5-2. Comparison of switching waveforms between TO-247-4L (SCT4036KR) and TO-247N (SCT4036KE)

Furthermore, Figure 5-3 shows the waveforms of switching losses *E*on and *E*off.

In TO-247-4L, the problem of delayed switching speed due to electricity generated in the source terminal is resolved, reducing the total switching loss by approximately 65%.

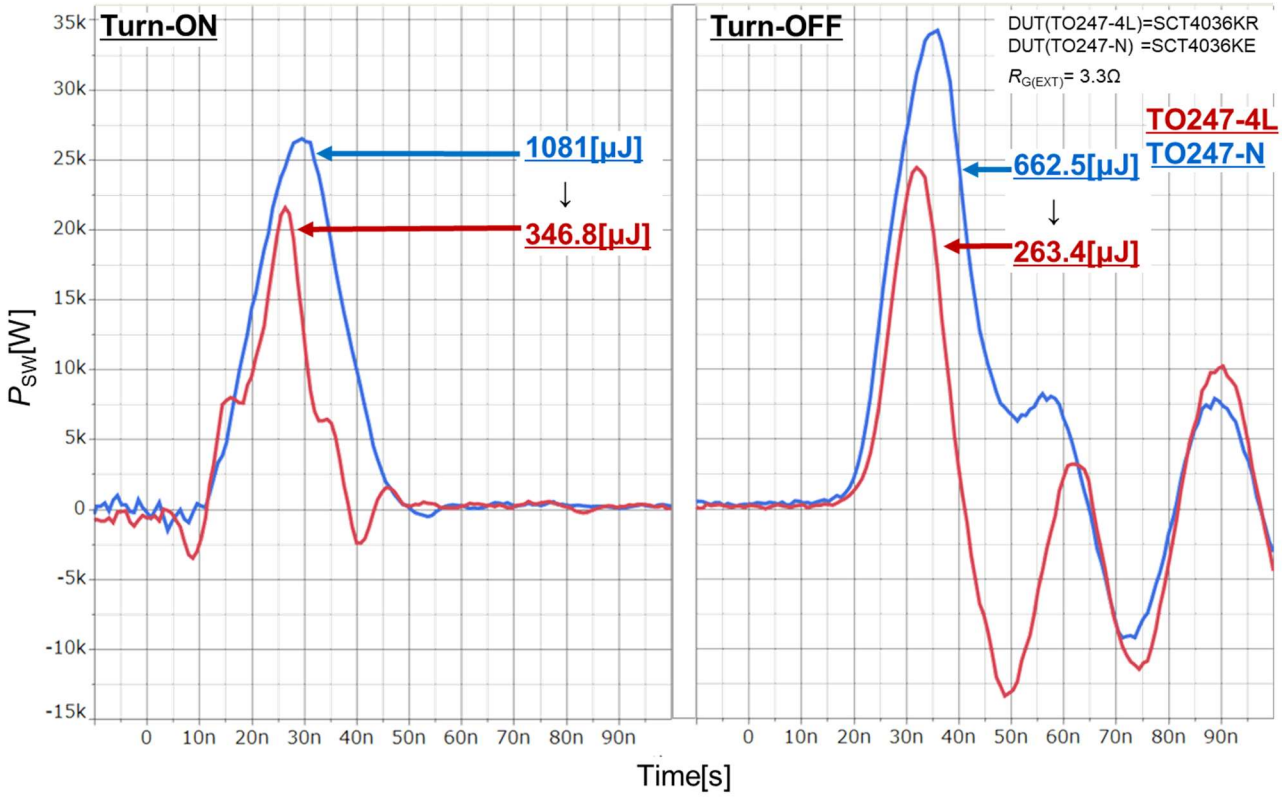


Figure 5-3. Comparison of switching losses between TO-247-4L (SCT4036KR) and TO-247N (SCT4036KE)

These results confirm that the switching loss can be reduced with the TO-247-4L package equipped with the driver source terminal compared with the normal TO-247N. The 4th Gen SiC MOSFETs can exhibit sufficiently excellent characteristics even in the TO-247N package. However, it can be used as a device with even lower loss in TO-247-4L by paying attention to the switching surge and other issues and referring to this application note to design the circuit appropriately.

6. Product lineup of 4th Gen SiC MOSFETs

For the product lineup of the 4th Gen SiC MOSFETs discrete packages, visit ROHM's website (the following URL)
https://www.rohm.com/products/sic-power-devices/sic-mosfet

7. Summary

We have shown that the 4th Gen SiC MOSFETs has advantages over previous products in the low loss, usability, and high reliability, and can solve customer design issues, such as improved system efficiency. Meanwhile, the dramatic improvement in the switching speed requires careful considerations of the circuit design to suppress the V_{GS} surge and the V_{DS} ringing during turn-off, covering the wiring inductance as well. We expect that this application note will help you use the 4th Gen SiC MOSFETs correctly and obtain its maximum performance.

References:

*1「SiC Power Devices and Modules Application Note Rev.003」
Application Note (No. 63AN102E Rev.003) ROHM Co., Ltd., November 2020

*2「Gate-source voltage behaviour in a bridge configuration」
Application Note (No. 60AN135E Rev.002) ROHM Co., Ltd., April 2020

*3「Gate-Source Voltage Surge Suppression Methods」
Application Note (No. 62AN010EJ Rev.002) ROHM Co., Ltd., April 2020

*4「Snubber circuit design methods」
Application Note (No. 62AN037E Rev.002) ROHM Co., Ltd., April 2020

*5「Improvement of switching loss by driver source」
Application Note (No. 62AN040E Rev.002) ROHM Co., Ltd., April 2020

*6「Precautions during gate-source voltage measurement」
Application Note (No. 62AP085E Rev.002) ROHM Co., Ltd., April 2020

*7「Calculating Power Loss from Measured Waveforms」
Application Note (No. 62AN134E Rev.002) ROHM Co., Ltd., June 2022

*8「Calculation of Power Dissipation in Switching Circuit」
Application Note (No. 62AN132E Rev.001) ROHM Co., Ltd., July 2020

*9「Method for Monitoring Switching Waveform」
Application Note (No. 62AN152E Rev.001) ROHM Co., Ltd., April 2020

*10「Importance of Probe Calibration When Measuring Power: Deskew」
Application Note (No. 63AN149E Rev.001) ROHM Co., Ltd., December 2020

*11「Impedance Characteristics of Bypass Capacitor」
Application Note (No. 63AN091E Rev.001) ROHM Co., Ltd., September 2020

*12「What Is Thermal Design?」
Application Note (No. 64AN031E Rev.001) ROHM Co., Ltd., June 2021

*13「Basics of Thermal Resistance and Heat Dissipation」
Application Note (No. 64AN043E Rev.001) ROHM Co., Ltd., August 2021

*14「Method for Calculating Junction Temperature from Transient Thermal Resistance Data」
Application Note (No. 64AN028E Rev.001) ROHM Co., Ltd., June 2021

*15「Notes for Temperature Measurement Using Thermocouples」
Application Note (No. 62AN154E Rev.001) ROHM Co., Ltd., April 2020

*16「Two-Resistor Model for Thermal Simulation」
Application Note (No. o. 62AN156E Rev.001 Rev.001) ROHM Co., Ltd., April 2020

*17「Notes for Temperature Measurement Using Forward Voltage of PN Junction」
Application Note (No. 62AN136E Rev.001) ROHM Co., Ltd., April 2020

*18「What is a Thermal Model?」
Application Note (No. 62AN105E Rev.001) ROHM Co., Ltd., December 2019
*19「How to Use Thermal Models」
Application Note (No. 64AN113E Rev.001) ROHM Co., Ltd., February 2020
*20「Measurement Method and Usage of Thermal Resistance RthJC」
Application Note (No. 63AN040E Rev.002) ROHM Co., Ltd., September 2022
*21「Precautions When Measuring the Rear of the Package with a Thermocouple」
Application Note (No. 63AN067E Rev.001) ROHM Co., Ltd., October 2020

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